Dedicated 4πβ (LS)-γ (HPGe) digital coincidence system based on synchronous high-speed multichannel data acquisition *

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Abstract: A dedicated 4πβ (LS) -γ (HPGe) digital coincidence system with five acquisition channels has been developed. Three ADC acquisition channels with an acquisition resolution of 8 bits and acquisition rate of 1 GSPS are utilized to collect the signals from three PMTs which are used to detect β decay, and two acquisition channels with an acquisition resolution of 16 bits and acquisition rate of 50 MSPS are utilized to collect the signals from high-purity germanium (HPGe), which is used to detect γ decay. In order to increase the accuracy of the coincidence system, all five acquisition channels are synchronous within 500 ps. The data collected by the five acquisition channels will be transmitted to the host PC through a PCI bus and saved as a file. Off-line software is utilized for the 4πβ (LS)-γ (HPGe) coincidence and data analysis as needed in practical applications. Tests of the system show that system can record pulse signals from 4πβ (LS) -γ (HPGe) synchronously for further coincidence calculation and the highest coincidence rate of the system is 20 K/s, which is sufficient for most applications. Compared with traditional coincidence modules like MAC3, the digital coincidence system has a higher flexibility of coincidence algorithm. In addition, due to the use of ADC, the structure of the coincidence system is simplified. This paper introduces the design of the hardware, the synchronization method and the test results of this system.

Keywords: liquid scintillation, 4πβ (LS) –γ (HPGe) coincidence system, high-speed ADC.

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1 Introduction

The 4πβ-γ coincidence counting method has been a major technique for radionuclide standardization for decades. As a direct activity measurement method, it can determine the activity without any quench indicating parameters, and the counting efficiency without a reference standard [1]. Traditional 4πβ-γ coincidence systems are composed of numerous electronic modules such as counting module, pulse shaping module, pulse-height analyzer and dead-time processing module. A traditional 4πβ (LS)-γ (HPGe) coincidence system consists of a counter module and MAC3 (Module d' Acquisition de Coincidences triples) which is used to get the coincidences of β pulse signals from three PMTs with analog devices, and is very inconvenient. So far, new techniques and digital coincidence systems have been applied for 4πβ-γ coincidence in various applications. ADCs (Analogue-to-digital converters) and FPGAs (Field Programmable Gate Arrays) have been applied widely in coincidence measurement to improve the performance of the coincidence system[1–3]. At the same time, most dedicated modules like the MAC3 and counter module have been implemented using FPGA logic [4–6]. ADCs are used by these digital coincidence systems to sample the signal of the 4πβ-γ system and the FPGA fulfils the function of coincidence.

Normal digital 4πβ-γ coincidence systems employ commercial acquisition cards to sample the radionuclide decay signal. Most of these cards sample the signal at a maximum speed of 25 MSPS (Million Samples per Second) which only meets the requirements of 4πβ-γ coincidence with a detector configuration of a sandwich type PS (plastic scintillator) or a type NaI (Tl) scintillation detector [4]. To achieve the primary activity measurements based on LS (Liquid Scintillation) such as 4πβ (LS) and TDCR (Triple to Double Coincidence Ratio), commercial acquisition cards with a higher acquisition speed, like 125 MSPS or 200 MSPS, are used [1,2]. The pulse width of the liquid scintillation, however, can be as low as 4 ns [7], so as the sampling interval of these coincidence systems is 5 ns, these pulses probably cannot be recorded. Although algorithms can be used to compensate for the measurement error, deviation is sometimes

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still introduced. In addition, normal digital 4πβ-γ coincidence systems cannot record an entire β pulse shape, so the shape analysis cannot play an efficient role in 4πβ (LS) coincidence. With the rapid development of ADCs, nowadays commercial acquisition cards can sample the signal from PMTs (photomultiplier tubes), which are used to detect beta decay directly with a sampling rate higher than 1 GSPS. Signals from HPGe (High Purity Germanium), which is used to detect gamma decay, can also be sampled directly by commercial acquisition cards with 16-bit sampling resolution, which have an advantage in the energy spectrum analysis. Commercial acquisition systems have the following deficiencies, however. Firstly, the signal generated by the PMT is a negative pulse, and the signal generated by the HPGe is a positive pulse. Commercial acquisition systems are usually unable to fit the input range of the signal, or they lose half of the ADC measurement range, as most commercial acquisition cards are designed to sample a bipolar signal. Secondly, 4πβ (LS)-γ (HPGe) needs three high-speed acquisition channels to sample the signal from the PMT and two normal speed acquisition channels to sample the signal from the HPGe, so we should have all the acquisition channels synchronous with the same timestamp to do 4πβ-γ coincidence [8]. It is hard to synchronize all the acquisition channels. Thirdly, to sample two different types of signals (β and γ signal), two kinds of acquisition cards should be used, but different acquisition cards usually have different working modes and output data formats, so it is hard to unify all the acquisition channels. In addition, the maximum rate of the coincidence events is up to 10000 per second, and choosing a suitable method to record so much data becomes difficult. Besides all the reasons above, a commercial acquisition card which is suitable for all the above-mentioned performance requirements is quite expensive, which will be a large obstacle in generalizing the use of the system.

Therefore, in this paper we introduce an in-house coincidence system based on FPGA and high-speed ADC. All the hardware of this system is designed by ourselves to fully satisfy the requirements of the 4πβ-γ coincidence system. Three high-speed acquisition channels can sample signal at a speed of 1 GSPS to record the pre-amplified PMT signal, and two normal speed acquisition channels can sample signal with a 16-bit resolution at a speed of 50 MSPS. All the information about the decay signals, such as amplitude and shape, will be recorded with no bias. The logical module in FPGA can fulfill the function of MAC3. Different from commercial cards, the acquisition channel of our system is synchronous within 500 ps, which can decrease the workload of the off-line software and increase the coincidence accuracy at the same time. The data sampled by the acquisition channels will first be processed by the FPGA, and then stored in DDR2 SDRAM for PCI conflict detection. All the data in DDR2 will transmitted to the host computer by PCI data bus to be processed off line, as shown in Fig. 1. In the test, we sampled ^{90}Sr LS signals and drew the wave from the data sampled by the high-speed acquisition channel. We also sampled the γ signal of ^{40}K generated by the HPGe detector and drew the energy spectrum.

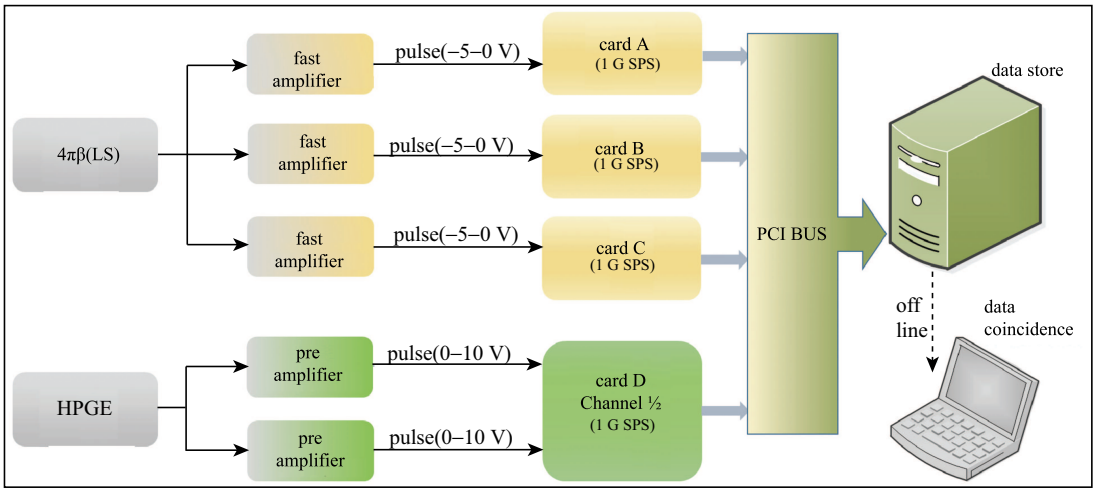

Fig. 1. (color online) Simplified block diagram of the 4πβ (LS)-γ (HPGe) digital coincidence system.

2 Data acquisition module

The basic structure of the coincidence system is shown in Fig. 1. In order to acquire the β signal, three acquisition cards, marked in yellow, are utilized to sample the signal generated by 4πβ (LS) with three PMTs. Moreover, the β signal is only amplified by the fast amplifier. Compared with traditional 4πβ (LS), it can not

only reduce the decay of the pulse signal but also decrease the conducted interference caused by other modules. The β signal from LS is a pulse with an amplitude of −5–0 V and a time width from 4 to 20 ns. To sample the signal directly, a sample rate up to 1 GSPS is needed. As the pulse has a 5 V margin, there should be a minimum voltage resolution of 0.1 V for applying the acquisition module to low-energy β nuclide, such as ^{3}H. In order to interface with the FPGA with a low cost, the data bus to FPGA should not have too high rate [9]. In fact, these are all achieved. TI ADC08D500 is chosen to support a sample rate up to 1 GSPS by cross sampling with the ADC08D500's two ADC channels. The chip's data interface supports 1:2 DEMUX & LATCH technique, which can turn the 8-bit data bus into a 16-bit bus for each ADC channel[10]. Compared with other 1 GSPS ADCs, this chip in this system has an acquisition rate of 1 GSPS at a data bus speed of 250 M. With the chip's DDR (Double Data Rate) LVDS (Low-Voltage Differential Signaling) data interface support, the data interface's clock to FPGA is 125 M, which can increase the stability of the FPGA. According to the final test, the ENOB (Effective Number Of Bits) of the 1 GSPS channel @ 250 MHz input is 7.2 (Signal generator: Tektronix AWG5000 series : 600 MS/s maximum sampling rate, 2.5 G bandwidth, 14-bit D/A resolution, 16 M memory length). Although it is lower than 7.5 as shown in the datasheet of the device [10], it can still meet the requirement of the minimum voltage resolution.

For the acquisition of the two channels of γ signal from HPGe, a normal-speed acquisition card with two ADC channels of 16 bits and 50 MSPS is utilized. As for the β signal, the pulse signal of the pre-amplifier is sampled. Its difference from the β signal is that the amplitude of the γ signal is 0−10 V and the time width of the γ signal is above 1 μs. As the γ signal is slower than the β signal, the acquisition rate of 50 M SPS is enough to sample the signal. In order to analyze the spectra of the γ nuclides, the minimum voltage resolution is quite important. As a result, ADI AD9268 is chosen. Tests of the acquisition channel show that the SNR (Signal-to-Noise Ratio) of the γ acquisition channel is 74.3 (the same as the signal generator) at 10 MHz, which is important for the spectral analysis of γ signals [11].

3 System channel synchronization

As shown in Fig. 2, three high-speed acquisition cards, marked in yellow, and one normal-speed acquisition card, marked in green, are plugged into the PXI (PCI extension for instrument) case. In order to let all the acquisition channels sample at the same timestamp, all the acquisition cards should operate under the condition of the same clock with a synchronous clock reset function. Fig. 3 shows the structure of the red card, which is utilized to synchronize the acquisition cards. The main function of this card is to distribute a reference clock of 50 MHz and send a synchronous reset signal called SYNC through the star-shaped trigger line on the PXI case. This card should be plugged into Slot 2 of the PXI case, as the star-shaped trigger line is only provided at this location. The star-shaped trigger line is a trigger with a time delay on the PXI case, which is utilized to send a SYNC clock reset signal to enable all the timestamps to be reset on each acquisition card. Therefore, the timestamps have not only the same reset but also the same time counter. The synchronization module of each acquisition card utilizes a 48 bit timestamp, which will not be repeated within 65 days. The time is long enough to meet most measurement requirements.

The reason for distributing a clock of 50 MHz is that the three acquisition cards with a sampling rate of 1 G SPS need a reference clock of 500 MHz, and the normal-speed acquisition card utilizes a reference clock of 50 MHz. Consequently, a reference clock of 50 MHz is the best choice to both increase time reliability and decrease the complexity of the synchronization module. In order to achieve the same delay time from each acquisition channel, cables with the same length are utilized. The clock of 50 MHz is sent by the front panel as shown in Fig. 2.

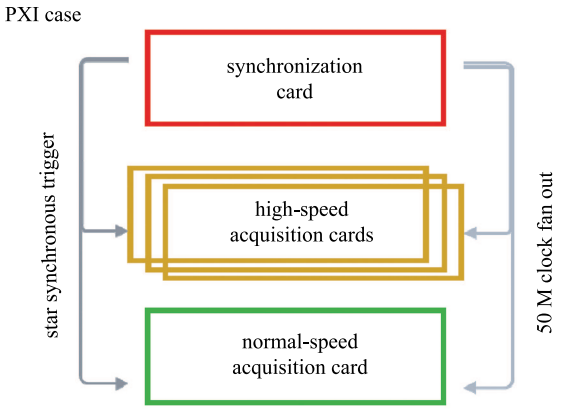

Fig. 2. (color online) PXI case with our coincidence system.

As the sampling interval of the high-speed acquisition channel is 1 ns, so the clock mismatch for all the high-speed acquisition channels is supposed to be within 500 ps, and the normal-speed acquisition channel should also be synchronous with the high-speed channels. To meet this requirement, a PLL (Phase Locked Loop) chip AD9524 is applied in the synchronization module shown in Fig. 3. The AD9524 can not only control the phase of the clock to obtain a clock mismatch within 500 ps, but also provide 4 fan-out low jitter LVDS clocks [12]. The synchronization between high-speed acquisition channels

and normal-speed acquisition channels can be adjusted by setting the parameters of this chip. It also provides 4 LVDS reference clocks to each acquisition card. As worked out with the oscilloscope (Agilent Infinii Vision 7000B), the average jitters of the 4 LVDS clocks to each card are 12.08, 12.38, 12.10 and 12.44 ps respectively. As the jitter will decrease the SNR of the ADC channels on the acquisition cards, each of the acquisition cards shall also utilize an AD9524 to eliminate the jitter. For the high-speed acquisition cards, the PLL is also utilized to multiply the clock frequency to 500 MHz.

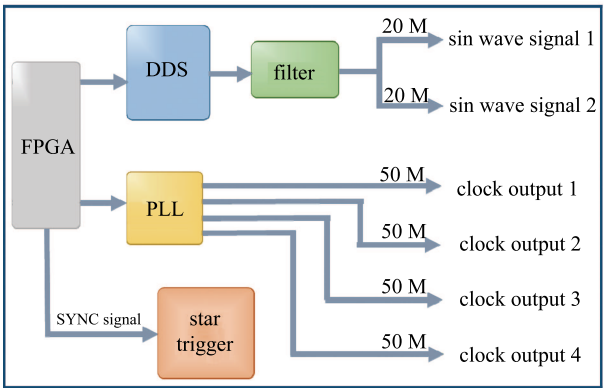

Fig. 3. (color online) Schematic diagram of the components of channel synchronization module.

To calculate the mismatch of each ADC channel, two 20 MHz sine waves are fanned out with a DDS (Direct Digital Synthesizer). The sine waves are filtered by utilizing a band-pass filter to improve the SNR. Each acquisition channel samples 4096 points from the sine waves at the same timestamp to calculate the phase. Then, a FFT (Fast Fourier Transform) function is used to calculate the phase.

A sine wave can be described as

$$F(\omega) = A(\omega) + \mathrm{j}B(\omega). \tag{1}$$

The initial phase can be described as

$$\theta = \tanh^{-1}(B(\omega)/A(\omega)). \tag{2}$$

If the acquisition channel A has the initial phase θ_{a}, and acquisition channel B has initial phase θ_{b}, then the phase difference between the two acquisition channels is

$$\Delta\theta = \theta_{\mathrm{a}} - \theta_{\mathrm{b}}. \tag{3}$$

After the adjustment of the PLL and the line, the average $\Delta\theta$/rad of each acquisition channel is 0.003. Then the mismatch of each acquisition channel is

$$\Delta T = (\Delta\omega T_{\omega})/(2\pi) = \frac{0.003}{2\pi} \times \frac{1}{20\times 10^6} = 0.02387 \text{ ns} \tag{4}$$

This result meets the requirements for the synchronization.

4 FPGA logic module

In order to reduce the complexity of the acquisition system design, all the acquisition cards have the same schematic diagram for the FPGA, as shown in Fig. 4. The only difference between the high-speed acquisition card and normal-speed acquisition card is the ADC interface schematic diagram of the FPGA and the ADC chip on each acquisition card. The ADC on high-speed acquisition card is ADC08D500, the interface for the ADC is 32 bit DDR LVDS data bus with a clock of 125 MHz; the ADC on normal-speed acquisition card is AD9524, the interface for the ADC bus is a 32 bit CMOS with a clock of 50 MHz. The data sampled by the ADC will first be screened to reduce the amount of data. When a signal is larger than the pre-set trigger line, a trigger signal will be generated. A rejection time is also set to meet the special requirement of data screening. The screening module will enable the write function of the ADC data FIFO (first in first out) if all the requirements on the data stream are met. A data package will be recorded into the FIFO to wait to be sent to the DDR2 SDRAM. The data package, as shown in Table 1, has 128 byte data or 256 byte data for selection. It can be set by the acquisition software to fit the length of the pulse. Most of the time, we use 128 byte data for β signal recording and 256 byte for γ signal recording.

All the data in the DDR2 SDRAM is transferred at a speed of 1 M bytes per DMA burst. The PCI also transfers the configuration command to configure the PLL device and ADC. When there are 10000 pulses per second, 8.75 Mbyte of data should be transferred (10000 × (3×128 byte + 2×256 byte)). Tests of the system show that the system is able to work very well at this pulse rate. According to the pressure test, it is found that the system can also work well at a pulse rate of 20000, which can also meet the requirements of most measurements.

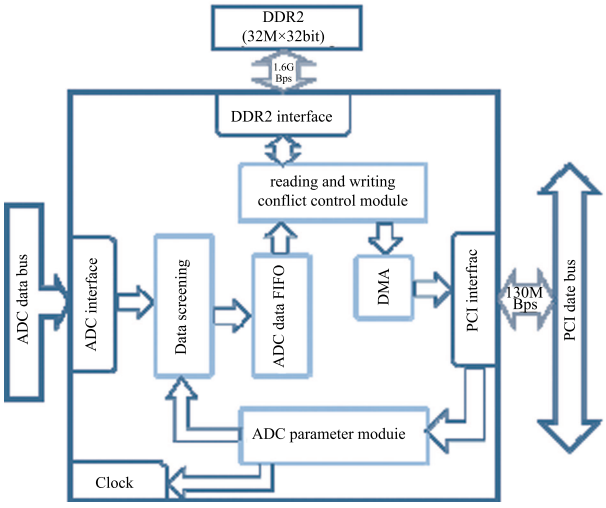

Fig. 4. (color online) Schematic diagram of the FPGA.

Table 1. Data package of the system.

data package(128 byte or 256 byte)			
channel number (1 byte)	extraction ration (1 byte)	time stamp (6 byte)	context (120 byte or 248 byte)

5 System testing

To test the coincidence system, we first used a signal generator (Tektronix AWG5000 series) to simulate the pulse signals generated by β and γ decay. As the AWG5000 only has two output channels, we used a channel to simulate the β decay and then fanned it out by the connector, doing the same for the γ decay. The β pulse had an 18 ns pulse width, and the amplitude of the pulse was −0.5 V shown by Fig. 5(a). The γ pulse had a 2 μs pulse width, and the amplitude of the pulse was 2 V shown by Fig. 5(c). The two channels were set to be externally triggered by a random trigger source. The trigger rate was 20 K/s. In the test, we found our system was working well, and all the pulses were recorded. A β pulse sampled by our system is shown in Fig. 5(b), and a γ pulse is shown in Fig. 5(d). Compared to the measurements from oscilloscope (Agilent Infinii Vision 7000B), we find it can well recover the shape of the pulse.

The real test environment was provided by the National Metrology Institute of China, with the 4πβ (LS) light chamber. To compare with the traditional coincidence system, we used Ultima Gold LLT as the liquid cocktail, and 6.59×10^3 Bq ^{3}H as the nuclide source. The signal from the PMTs was fanned out to the traditional MAC3 and our system. The trigger line was set as −60 mV. As shown in Table 2, our system can fulfil the function of the traditional coincidence system.

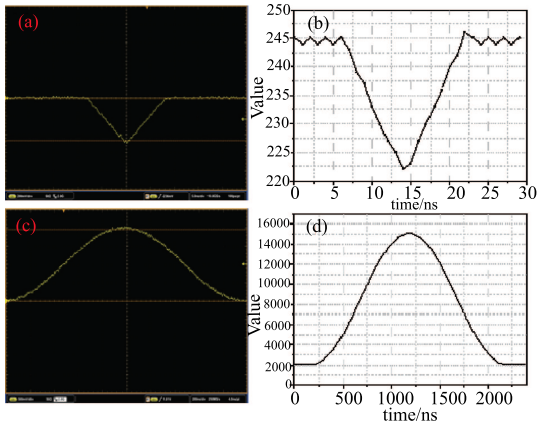

Fig. 5. (color online) (a) Simulated β pulse sampled by oscilloscope; (b) Simulated β pulse sampled by our system; (c) Simulated γ pulse sampled by oscilloscope; (d) Simulated γ pulse sampled by our system.

Table 2. Test result compared with MAC3.

device	time/s	counter per second	efficiency
MAC3	45	3455	52%
our system	45	3455	52%
MAC3	4500	3457	52%
our system	4500	3457	52%

To show the ability of the β shape recording, we used Ultima Gold AB as the liquid cocktail, ^{90}Sr as the nuclide source. Three high-speed acquisition channels were used to sample the β signals from ^{90}Sr. Fig. 6(a) shows the pulses drawn by the sampled data.

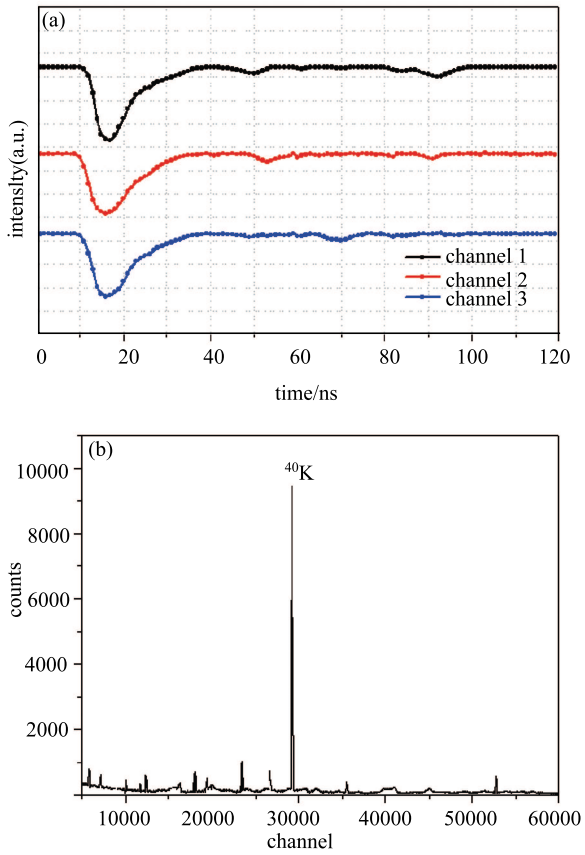

Fig. 6. (color online) (a) β pulse shapes sampled by three high-speed acquisition channels in measurement of ^{90}Sr; b) ^{40}K energy spectrum drawn by our system.

It seems that the system can record the β signals synchronously in a real experimental environment.

For the γ test, we used ^{40}K as our nuclide source, giving the energy spectrum of ^{40}K shown in Fig. 6(b). The line around channel 30000 indicates the ^{40}K peak. The small peaks of this spectrum are attributed to contamination from other radionuclides. We find that our system can draw the energy spectrum precisely.

6 Conclusion

In this paper, a 4πβ (LSC) -γ (HPGe) coincidence system is presented. Tests show that the hardware and the software designed can work well to reach the requirements of 4πβ (LSC) -γ (HPGe). Further tests will be done to find more methods of radionuclide measurement using this coincidence system.

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