Chinese Physics C Vol. 38, No. 10 (2014) 106101

Development of a multi-channel readout ASIC for a fast neutron spectrometer based on GEM-TPC[*]

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Abstract: A multi-channel front-end ASIC has been developed for a fast neutron spectrometer based on Gas Electron Multiplier (GEM)-Time Projection Chamber (TPC). Charge Amplifier and Shaping Amplifier for GEM (CASAGEM) integrates 16+1 channels: 16 channels for anodes and 1 channel for cathode. The gain and the shaping time are adjustable from 2 to 40 mV/fC and from 20 to 80 ns, respectively. The prototype ASIC is fabricated in 0.35 μm CMOS process. An evaluation Print Circuit Board (PCB) was also developed for chip tests. In total 20 chips have been tested. The integrated nonlinearity is less than 1%. The equivalent noise electrons is less than 2000e when the input capacitor is 50 pF. The time jitter is less than 1 ns. The design and the test results are presented in the paper.

Key words: front-end, readout electronics, ASIC, TPC, GEM

PACS: 29.40.Cs, 29.30.Hs **DOI:** 10.1088/1674-1137/38/10/106101

1 Introduction

The fast neutron spectrometer has been widely used as a diagnosis tool for basic nuclear physics experiments and many other application fields such as nuclear reactor monitoring. A proton recoil type neutron spectrometer based on GEM (Gas Electron Multiplier)-TPC (Time Projection Chamber) has been proposed [1]. Benefiting from its capability of measuring three dimensional proton tracks, this novel detector can achieve high detection efficiency and excellent neutron/gamma (n/γ) discrimination power.

In order to measure the proton tracks with good precision, the charge collection electrode is divided into small pads in millimeters. The cluster position is then derived from the center of gravity (COG) of the induced charge. The third dimension is estimated from the electron drift time with precision in tens of nano-seconds [1]. Two dimensional pads are used since there are usually multi-clusters in one track, requiring very high density readout electronics [2–5]. A dedicated front-end ASIC has been developed for the GEM-TPC for fast neutron measurement. It consists of a preamplifier and a $CR-(RC)^5$ shaper for each channel and can directly drive a 50 Ω load, which is very convenient for sending the outputs to fast waveform digitizers. Energy and timing information can be extracted from the waveforms.

The specifications of the chip will be shown in Section 2. The requirements of the detector will also be shortly introduced. Detailed circuit design and test results will be described in Section 3 and Section 4 respectively.

2 Requirements and specification

The specifications of the ASIC are shown in Table 1. The pad size is chosen to be 2 mm×5 mm, which is a trade-off between the detector efficiency and the density of the readout electronics [1]. In total 720 channels are required to read out a 10 cm^2 detector area. The pad signals are connected out by flexible cables with 16 channel signals each. Hence the first prototype ASIC has integrated 16 channel front-end circuits for anode pads. An additional cathode readout channel was also implemented to generate a trigger signal. The power consumption of each channel is less than 10 mW.

Table 1. The specifications of CASAGEM.

element	value	unit	note
gain	2, 4, 20, 40	mV/fC	
dynamic range	0–1000	fC	
shaping time	20,40,60,80	ns	
integrated linearity	<1%		
power consumption	<10	mW/ch	
ENC	<2000	electron	input cap:50pF

Received 5 November 2013, Revised 25 February 2014

[*] Supported by National Natural Science Foundation of China (11275109)

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The pad signal can be up to 1 pC for a typical double layer GEM configuration for neutron energy up to 5 MeV. The gain of the ASIC is adjustable from 2 mV/fC to 40 mV/fC. It satisfies the maximum 1 pC dynamic range and also provides the flexibility for detector optimization in the future.

The energy resolution of the neutron is directly dependent on the resolution of the total energy deposited in the detector by the recoil proton and the angle resolution of the proton track, which makes it difficult to find an optimized trade-off between the noise and the shaping time of the ASIC. Two measures were used to address this issue: 1) the shaping time of the ASIC is adjustable from 20 ns to 80 ns; 2) the waveform sampling approach was adopted and the amplitude and timing information can be extracted by different digital signal processing algorithms. By using full wave integration, the ballistic deficit won't affect the energy measurement. The noise of the preamplifier is optimized for 50 pF and 100 pF input capacitance for the anode channel and cathode channel respectively. Considering the noise performance, the shaping time of this ASIC is chosen 80 ns. As the ASIC incorporates a $CR-(RC)^5$ shaper, the peaking time of the output signal is 400 ns.

3 Circuits design

The block diagram of the anode and the cathode channels are shown in Fig. 1 and Fig. 2. Each channel consists of a charge sensitive preamplifier, a $CR-(RC)^5$ shaper and a class-AB buffer. The first stage of the shaper is inverting for the anode channel and non-inverting for the cathode channel. So the output polarities are the same for both channels. The cathode channel also has a discriminator to generate a trigger signal.

3.1 Charge sensitive amplifier

The charge amplifiers are composed of two step amplifiers: a low noise preamplifier and an amplifier used to amplify the charge signal. The structure diagram of the low noise preamplifier is shown in Fig. 3. The preamplifier adopts the single ended cascode structure. The p-channel MOSFET is used as the reset device instead of resistance for reducing the noise and the layout area. For eliminating the effect of the MOSFET' s nonlinearity, the continuous compensation circuit is adopted [6].

3.2 Shaper

Both the anode readout channels and the cathode readout channel integrate a $CR-(RC)^5$ shaper. The

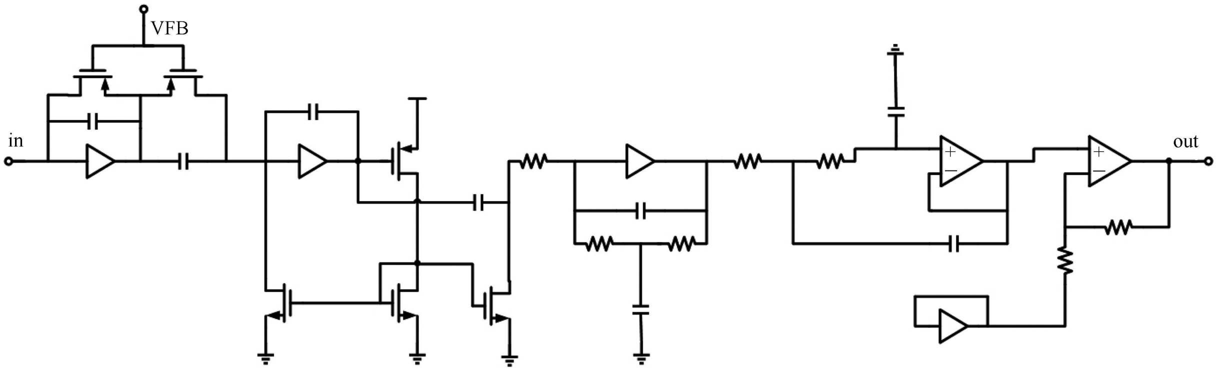

Fig. 1. Anode readout circuit diagram.

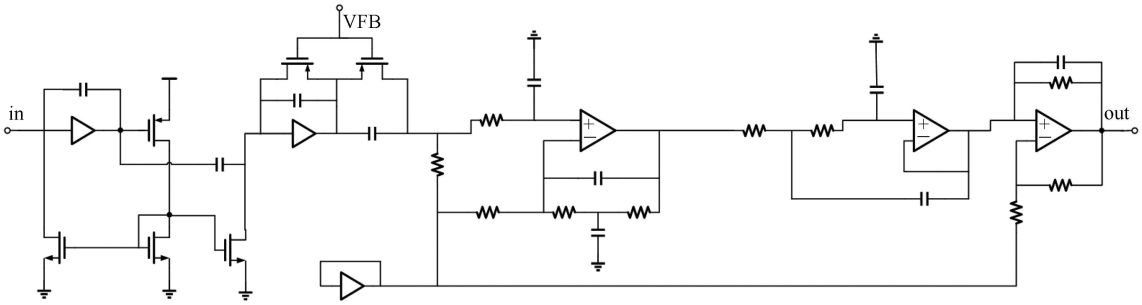

Fig. 2. Cathode readout circuit diagram.

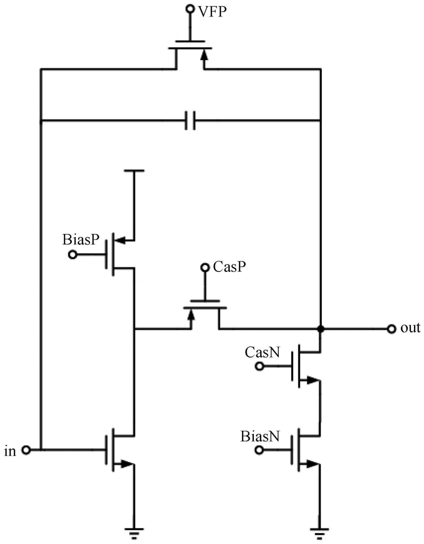

Fig. 3. The Preamplifier circuit diagram.

shaper consists of two stages: a T bridge filter and an SK filter. The shaping time can be set by adjusting the feedback resistors.

3.3 Buffer

The buffer uses a class-AB structure as its output stage to drive a high capacitive load and a 50 Ω load. It only consumes 3 mW of static power consumption. Therefore the ASIC can drive a long cable and fast wave digitizer easily. There is a dummy amplifier used to subtract the baseline for preventing the buffer from amplifying the baseline as well. The die area is 3 mm×3 mm. The layout is shown in Fig. 4 and the die is packaged in 121-pin BGA.

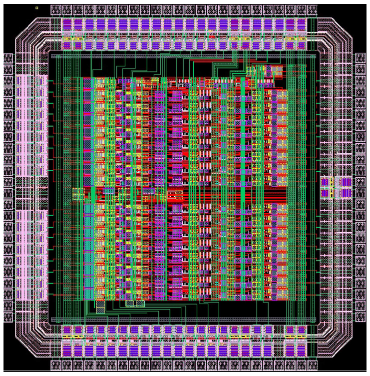

Fig. 4. The layout of CASAGEM.

4 Experimental results

CASAGEM has already been fabricated and tested. The test results will be presented in this section. This section includes 3 parts: function test, batch test, and energy spectrum test.

A dedicated evaluation PCB has been developed, as shown in Fig. 5. It uses BAV199(Philips) to protect the input MOSFET from the spark of the gas detector. The Dual In-line package (DIP) switch is used to set the ASIC's gain and shaping time.

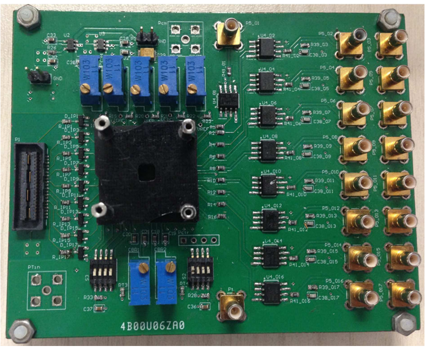

Fig. 5. The testboard of CASAGEM.

4.1 Funtion test

This test includes a gain linearity test, noise test and time jitter test. The ASIC can be set to 4 different gain and shaping times. According to the GEM-TPC requirements, the gain needs to be set as 4 mV/fC and the shaping time needs to be set as 80 ns.The test pulse is generated by using capacitance to pump the charge when step pulse gets through.

As shown in the readout circuit diagram, one readout channel integrates a pre-amplifier, two shaping amplifiers and a buffer. So the output node of the pre-amplifier, each output node of the shaping amplifiers and the output node of the buffer are chosen as the key nodes for studying the performance of one channel. The simulation waves of those four key nodes are shown in Fig. 6. For the pads of one dye are limited, only the buffer output

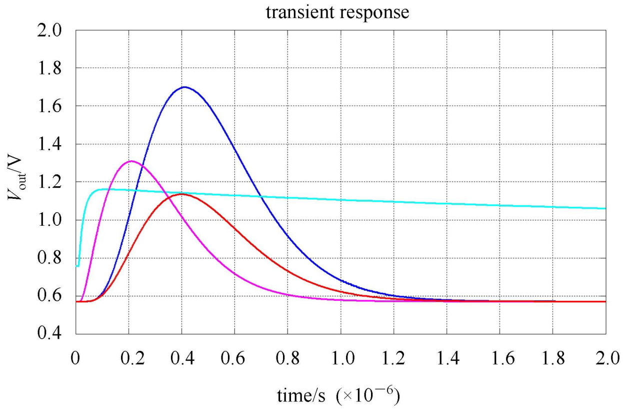

Fig. 6. (color online) The simulation waves of one readout channel. The cyan curve is the pre-amplifier output wave; the magenta curve is the first shaping amplifier output wave; the dark red curve is the second shaping amplifier output wave; the blue curve is the buffer output wave.

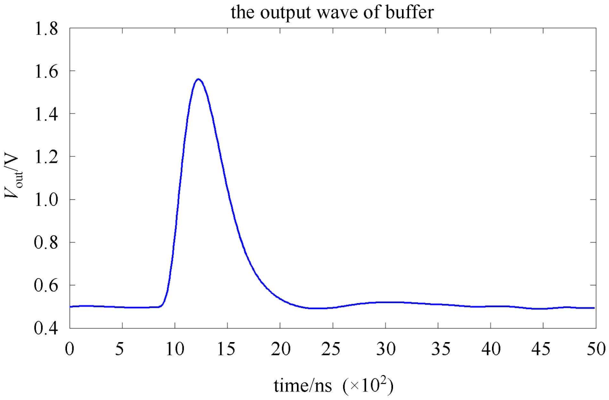

Fig. 7. The buffer output wave gotten by the fast ADC model (CAEN V1724).

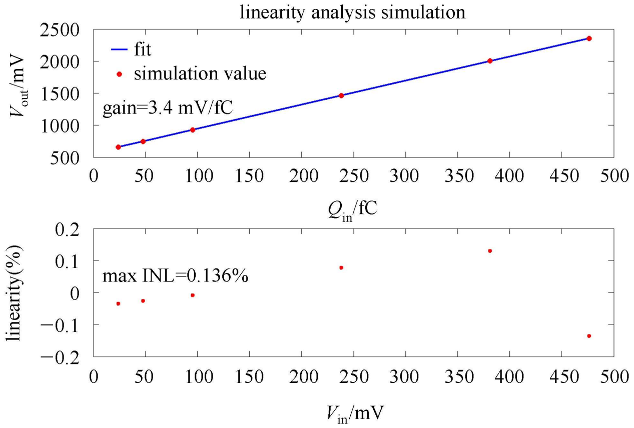

Fig. 8. The gain linearity simulation results. The ASIC gain is set to be 4 mV/fC and the ASIC shaping time constant is set to be 80 ns. The maximum integrated nonlinearity error is about 0.136%.

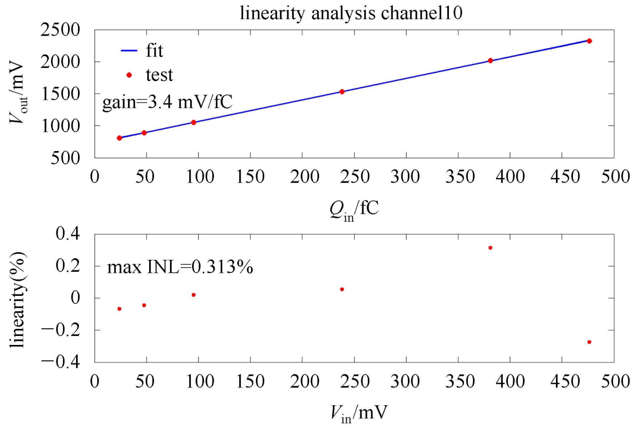

Fig. 9. The gain linearity test results. The ASIC gain is set to be 4 mV/fC and the ASIC shaping time constant is set to be 80 ns. The maximum integrated nonlinearity error in this condition tested is about 0.313%.

has an outlet pad. So only the buffer output wave has been recorded. The test wave is shown in Fig. 7. The simulation wave baseline is about 570 mV and the test wave baseline is about 540 mV. The simulation wave rise-time is about 404 ns and the test wave rise-time is about 420 ns. The parasitic capacitors and resistors make the circuit slow.

The gain and linearity simulation results are shown in Fig. 8.The gain linearity test results of one channel are shown in Fig. 9. The test gain is almost the same as the simulation gain. The test INL is slightly bigger than the simulation INL.

The noise performance of CASAGEM is measured by an oscilloscopen (Tektronix DPO 4034). The noise is tested by measuring the root-mean-square (RMS) of the CASAGEM output when it is powered up but no input signals inject. The noise slop is tested by measuring the different noise performance when adding different capacitors (10 pF, 22 pF, 47 pF, 100 pF) at the input of CASAGEM.

The noise tests results and simulation results are shown in Fig. 10. The shaping time is set as 80 ns. The circles show the measured ENC values; the squares show the simulation ENC values. The measured noise slop is about 20.95 e/pF. The simulation noise slop is only 6.178 e/pF. The cause of the notable difference is from the resistance between the input MOSFET's substrate and ground. Considering the substrate resistance effect, the simulation results shown as triangles are much closer to the measured values. The simulation noise slop when considering the substrate resistance effect is about 20.59 e/pF.

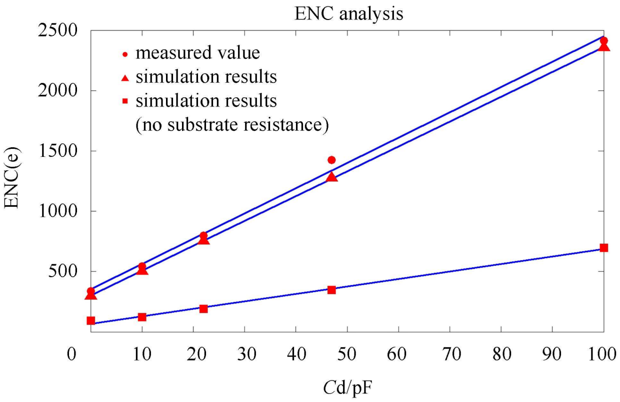

Fig. 10. Equivalent noise charge (ENC) as a function of the input capacitance.

The constant fraction timing is adopted to achieve the time information, so the time jitter of signal will affect the precision of the proton track measurement. The time jitter test results are shown in Fig. 11. The time spectrum is acquired by counting the time period between the test signal generated from the signal generator and CASAGEM output signal of which time information is gotten by constant fraction timing. The shaping time of CASAGEM is set as 80 ns. The test results show the time resolution is 517.8 ps.

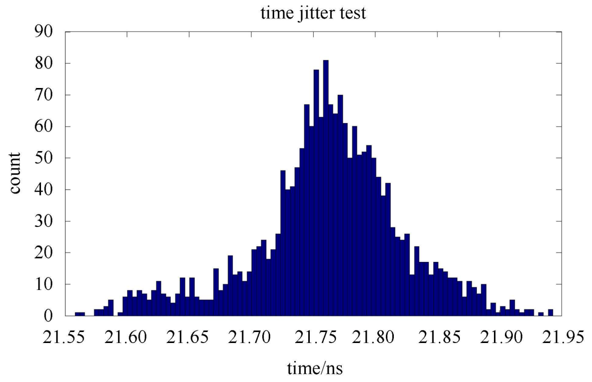

Fig. 11. The time jitter test results.

4.2 Batch test

Disposing of the chips damaged when packing and the chips tested before, there are 20 chips left to be tested. As the GEM-TPC needed, the gain is set to be 4 mV/fC and the shaping time is set to be 80 ns. The data acquisition system uses a 32 channel multi-event peak sensing ADC (CAEN V785) to acquire peak information and covert it to digital signals. The test statistical results are summarized in Table 2. All channels of these 20 chips tested work properly. The Fig. 12 is showing the gain statistical distribution. The inconsistency of the calibration capacitances will degrade the test results as well.

Table 2. Results of 20 chips test.

parameter	mean	max	min	Std
gain/(mV/fC)	3.38	3.56	3.22	0.074
baseline/mV	604	641	569	14.1
ENC(e)	1055	1743	734	118.4

4.3 Energy spectrum test

CASAGEM is used as the front end readout electronics of a GEM detector to study the energy spectrum of ^{55}Fe. The data acquisition system to digitize the CASAGEM signal is CAEN model V785.

The detector sets a two level GEM. The sensitive area of GEM is 5 cm×5 cm. The detector adopts two dimension readout strips. The readout strips are arranged perpendicularly. The energy spectrum is achieved by summing the signal of each strip and the trigger signal is gotten from the foil. Fig. 13 shows the test results. The energy resolution of the ^{55}Fe is about 25.7%(FWHM). The ration of full energy peak and the escape peak is 2:1 and the ration of full energy peak counts and the escape peak counts is 4:1.

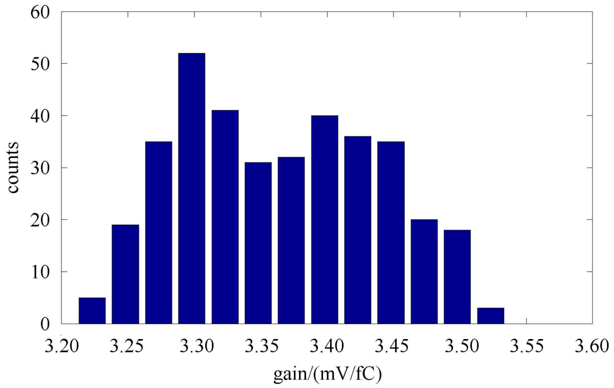

Fig. 12. The gain statistical distribution.

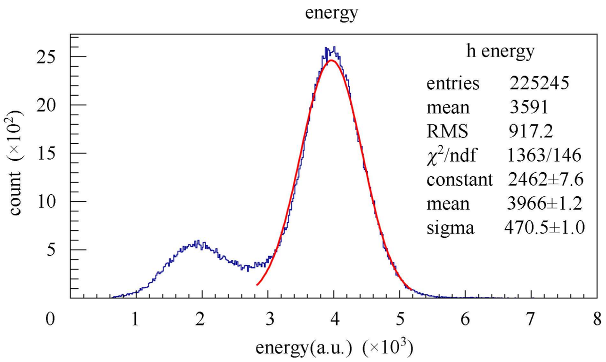

Fig. 13. Energy spectrum of the ^{55}Fe base on the CASAGEM.

5 Summary

An ASIC for GEM-TPC has been developed and tested. The specification can satisfy the requirement of the detectors. The first batch of chips have been tested and all the channels tested can work properly which shows this ASIC gets a high yield. More chips have been fabricated already. They will be used as the front-end readout electronics of neutron TPC.

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