Digital prototype of LLRF system for SSRF*

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Abstract This paper describes a field programming gate array (FPGA) based low level radio frequency (LLRF) prototype for the SSRF storage ring RF system. This prototype includes the local oscillator (LO), analog front end, digital front end, RF out, clock distributing, digital signal processing and communication functions. All feedback algorithms are performed in FPGA. The long term of the test prototype with high power shows that the variations of the RF amplitude and the phase in the accelerating cavity are less than 1% and 1° respectively, and the variation of the cavity resonance frequency is controlled within ±10 Hz.

Key words LLRF controller, field programming gate array, feedback algorithm, clock distribution, local oscillator

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1 Introduction

With the development of the large scale integrated circuit, digital technology is an option of the choice to build low level controller for the accelerator[1—3]. Its core consists of the high speed Field Programmable Gate Array (FPGA), and high speed ADC and DAC.

Shanghai Synchrotron Facility (SSRF) is a 3.5 GeV, 300 mA, the third generation synchrotron light source. It includes the 100 MeV linac, the booster, in which the beam energy will be ramped from 100 MeV to 3.5 GeV, and the storage ring.

The RF system includes three RF stations. Each has one superconductive cavity, one klystron and one set of LLRF control system only in storage ring. The RF system will have to provide 4 MV accelerating voltage and restore up to 600 kW power to the electron beam.

The digital LLRF control system includes two basic feedback loops: the field control loop (relative to the traditional amplitude and the phase feedback loop) to regulate the amplitude and phase of the RF field and the tuning feedback loop to compensate for the transient beam loading, the ripples of the high voltage power supply and the temperature variations. It requires controlling the amplitude and the phase within ±1% and ±1° in SSRF, respectively. The frequency adjusting is within ±10 Hz.

2 Overview of the block diagram

Figure 1 shows the feedback loop block diagram. In the prototype, the function block includes the local oscillator (LO) signal, the analog front end, the digital front end, the RF out, the clock signal distribution and the communication between the controller and the host PC.

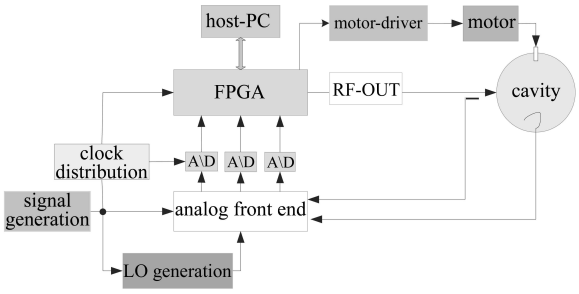

Fig. 1. Block diagram of feedback control loop.

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3 Hardware

The prototype hardware of low level RF system includes the LO signal, the clock signal distribution, the analog front end, the digital front end and the RF out.

We adopt direct digital synthesizer to obtain the LO signal instead of the Phase Lock Loop (PLL). The AD9858, which is the key component in LO generation, is a direct digital synthesizer (DDS) featuring a 10-bit DAC operating up to 1GSPS. The phase noise is less than 145 dBc/Hz @1 kHz when the output frequency is 100 MHz (DAC output). In practice, we first get the signal of 38.4 MHz through AD9858，and then use this signal mixing with the signal from the signal generator to get the LO signal.

The AD9510, which is used for the clock signal distribution, provides 122.88 MHz for the DAC converter and 30.72 MHz for the ADC converter. Moreover, both of them are sent into the FPGA as clock of digital signal processing. The total jitter of the clock is about 30 ps. The crystal oscillator is used for the communication clock whose frequency is 50 MHz.

The analog front end processes three signals: the reference signal (from the signal generator), the forward signal from waveguide, and the cavity signal from the pick-up. They are down-converted to IF (38.4 MHz) signal in this part.

At the digital front end, the chief components are three ADCs, one FPGA and one DAC. The ADC has two types, two of them are AD9433, and the other one is AD6645. They receive the analog IF signals from the analog front end and then translate them to digital signals for processing. The FPGA is Stratix II EP2S60 from Altera company. The field control and tune loop algorithm are done in this FPGA. And the LLRF self-interlock is included in the FPGA. In addition to the above main functions, the FPGA also provides the host pc with the interface, the registers and the PWM signal for driving the step motor.

In the RF out, the primary purpose is to translate the 38.4 MHz base-band control signals from the digital front end from digital to analog signals and then up-convert them to the RF frequency. It makes sure that the recovered signals have the dynamic range of 30 dB (−30—0 dBm).

LLRF control box assembled consists of three layers. The bottom layer is the power supply. The middle layer includes the hardware of the digital front end, the LO signal and the clock signal distribution. The analog front end and RF out are settled down on the top layer.

4 The algorithm

The equivalent circuit of the cavity is RLC parallel circuit. The transfer function[4] is:

$$C(S)=\frac{2\sigma RS}{S^2+2\sigma S+\omega_{\mathrm{R}}^2}\ , \tag{1}$$

where S is Laplacian, ω_{R} is the resonant frequency (rad/s) of the circuit, $\omega_{\mathrm{R}}=1/\sqrt{LC}$, σ is the damping rate (s^{-1}), $\sigma=\omega_{\mathrm{R}}/2Q$, and Q is the quality factor $Q=R\sqrt{C/L}$. In case of a carrier centered at the resonance frequency of the cavity, the transfer function is simplified to classical first-order low-pass filter responses:

$$C(S)=\frac{\sigma R}{(S+\sigma)}\ . \tag{2}$$

The feedback model of the cavity transfer function is showed in Fig. 2. In the model, it absorbs the forward delay (T_{F}) and reverse-delay (T_{P}) which limit the gain of loop. In the ideal situation, controller zero cancels cavity pole at $\sigma=K_{\mathrm{i}}/K_{\mathrm{P}}$, $K_{\mathrm{i}}=\pi/4(T_{\mathrm{F}}+T_{\mathrm{P}})$[5]. K_{i} and K_{P} are the gain value of the integral and proportional in PI algorithm respectively. Using this model, we can simulate the stability of the feedback loop and estimate how large the K_{i} and K_{P} are.

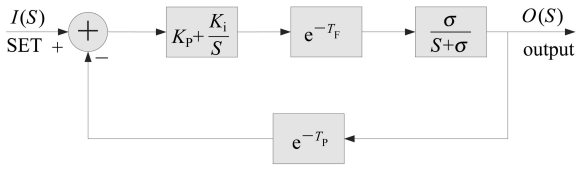

Fig. 2. Model of the transfer function.

The ratio of IF to the sample clock is 5/4 in our case. The phase difference is 90 degrees when they are converted into one period, so the data sequence is $I/Q/-I/-Q\cdots$, where $I=A\cos\theta$ (In-phase), $Q=A\sin\theta$ (Quadrature)[6]. Here, A and θ are the signal amplitude sampled and the instantaneous phase of the time of sample, respectively. The stabilities of the amplitude and phase are obtained through stabilizing the I and Q component of the cavity signal.

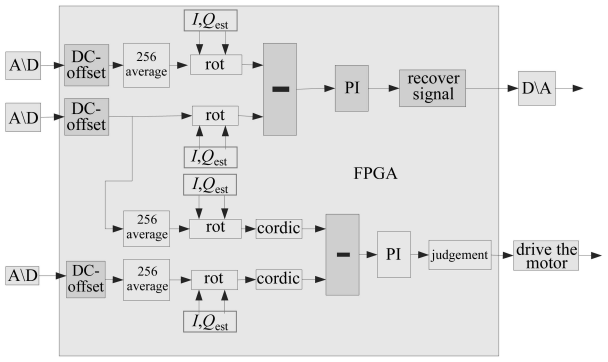

Fig. 3. Algorithm signal flow in FPGA.

The algorithm signal flow in FPGA of the field feedback control and tuning feedback loop is listed in Fig. 3. Proportional-integral is used in both of them.

It spends 9 clock cycles to do the field feedback control. In tuning the feedback loop, the tuning phase error of the cavity is calculated by using the CORDIC arithmetic[7]. The precision of detecting phase is 0.1°.

5 Results

The total responsive time of the field feedback loop is 1.5 μs. 660 ns is from the cable, the klystron and the cavity. The responsive time of controller (the analog front end, the digital front end and the RF out) is about 880 ns. In order to test the performance of the field control feedback loop, we add the phase and amplitude modulation. The modulation index is 30%, and the modulation frequency is from 465 Hz to 20 kHz. We obtain the different suppression corresponding different modulation frequency, from which we obtain the loop band width about 8 kHz as shown in Fig. 4. We have also measured the long-term stability of phase and amplitude. The result is showed in Fig. 5. The variations of the amplitude and phase are less than 1% and 1° , respectively. In proceeding the test, the tuning feedback loop is closed too, which can trace the resonance frequency variation because of the temperature and ripples of the high voltage power supply. The threshold of the phase error is set 0.3°. For the superconductive cavity (e_x=1.8×10^5), it is related to 7 Hz. The response of the tuning feedback loop is less than 1 ms.

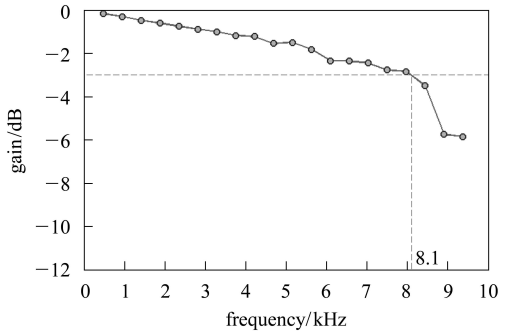

Fig. 4. The band width of the close loop.

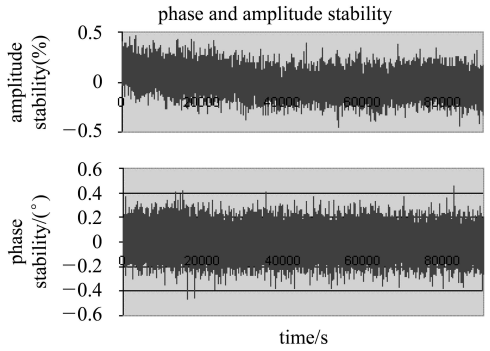

Fig. 5. Long-term stability of the amplitude and phase.

6 Future plan

There exist some problems for the commercial products. For example, the controller is not compact, and can not obtain higher control precision. The operation is complicated, and so on. So we will develop a custom board for the SSRF, which assembles the hardware mentioned above by using the Integral-Circuit.

7 Conclusions

We develop the digital low level RF controller for the SSRF based on the commercial digital boards. Through the high power and long term testing, the performance can satisfy the requirement on the accuracy of the amplitude, phase and resonance frequency of SSRF. The formal LLRF system will be obtained through copying this prototype.

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