System design for precise digitization and readout of the CSNS-WNS BaF_2 spectrometer*

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Abstract: The BaF_2 (barium fluoride) spectrometer is one of the experiment facilities at the CSNS-WNS (White Neutron Source at China Spallation Neutron Source), currently under construction. It is designed to precisely measure the (n, γ) cross section, with 92 crystal elements and complete 4π steradian coverage. In order to improve the precision of measurement, in this paper, a new precise digitization and readout method is proposed. Waveform digitizing with 1 GSps sampling rate and 12-bit resolution is used to precisely capture the detector signal. To solve the problem of massive data readout and processing, the readout electronics is designed as a distributed architecture with 4 PXIe crates. The digitized signal is concentrated to the PXIe crate controller through a PCIe bus on the backplane and transmitted to the data acquisition system over gigabit Ethernet in parallel. Besides, the clock and trigger can be fanned out synchronously to every electronic channel over a high-precision distribution network. Test results show that the prototype of the readout electronics can achieve good performance and meet the requirements of the CSNS-WNS BaF_2 spectrometer.

Keywords: CSNS-WNS BaF_2 spectrometer, readout electronics, waveform digitizing, clock and trigger network

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1 Introduction

The neutron radiation capture cross section, that is the (n, γ) cross section, is used to describe the probability of a radiation capture reaction between an incident neutron and a target nucleus. It is an important nuclear parameter, and plays a key role in the study of nuclear astrophysics, nuclide origin theory, nuclear energy development and nuclear waste disposal [1].

A 4π steradian detector composed of BaF_2 crystals is regarded as the best way to measure the (n, γ) cross section. Several BaF_2 detectors with 4π steradian have previously been constructed, including the barium fluoride detector (BFD) at Karlsruhe, Germany [2], the detector for advanced neutron capture experiment (DANCE) at Los Alamos National Laboratory, USA [3], the total absorption calorimeter (TAC) at CERN [4] and the gamma-ray total absorption facility (GTAF) at the China Atomic Energy Science Research Institute [5]. With these facilities, the (n, γ) cross sections of many nuclides were obtained and significant contributions were made to nuclear research and applications.

In China, an advanced spallation neutron source called the China Spallation Neutron Source (CSNS) is under construction in Dongguan. It will produce a wide band pulsed neutron beam, which is perfect for nuclear data measurement [6]. So a new white neutron source (WNS) pipe is being constructed in the opposite direction to the proton beam at CSNS and a new 4π steradian BaF_2 detector, namely the CSNS-WNS BaF_2 spectrometer, is being planned to measure the (n, γ) cross section. The CSNS-WNS BaF_2 spectrometer will be composed of a neutron pipeline, sample room, neutron absorber, BaF_2 crystals and photomultiplier tubes (PMTs) from inside to outside. It will contain 92 BaF_2 crystals. Each crystal is coupled with an ultraviolet sensitive PMT for photoelectric conversion. The BaF_2 spectrometer signal will have a wide energy range from tens of keV to 10 MeV, and wide frequency distribution from hundreds of Hz to about 120 MHz.

To precisely measure the (n, γ) cross section, the neutron time of flight, and the energy and multiplicity of the gamma rays should be measured and read out. Moreover, to filter out background signals caused by alpha

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particles in the BaF_2 crystal, pulse shape discrimination methodology (PSD) is used in the electronics. The gamma ray pulse shape should be captured precisely, and from this, gamma rays excited by neutrons can be recognized correctly. In the CSNS-WNS BaF_2 spectrometer, for each electronics channel, the dynamic range in amplitude reaches up to 500 times (from 4 mV to 2000 mV), energy resolution is better than 1% at 662 keV and time resolution is better than 1 ns. The neutron pulse beam of the CSNS-WNS has a frequency of 25 Hz and the event rate for the BaF_2 spectrometer is about 3 kHz. To sum up, large dynamic range, high energy and time resolution, high data rate and low dead time should be achieved for the readout electronics of the BaF_2 spectrometer. Besides, the readout electronics should also be compact and stable.

To read out the BaF_2spectrometer signal, BFD used traditional electronics, measuring energy by analog integration with peak-sampling and measuring time by a constant fraction discriminator (CFD) [2]. Each detector channel (42 for BFD) needs two electronic channels to deal with the fast and slow components of the gamma rays respectively. Too many electronic modules, such as linear gates, CFDs, attenuators and amplifiers, make the BFD electronics very complicated and not suitable for the CSNS-WNS BaF_2 spectrometer. For the DANCE [7], TAC [8] and GTAF [9] experiments, commercial compact PCI digitizer (flash ADC) modules are adopted to capture the detector waveform. However, the digitizing resolution for these experiments is 8 bits and the typical sampling rate is only 500 MHz, which cannot meet the requirements of large dynamic range and high-precision pulse shape discrimination. Actually, commercial modules focus on data acquisition, not on processing, which means the trigger and algorithm cannot be implemented in hardware and so the real time performance is limited. Besides, limited by the commercial modules, compact PCI platforms are used in these experiments. Data from the digitizers should be transmitted to the crate controller one by one through the shared PCI bus on backplane. The burst data rate is only 1056 Mbps. For applications with more channels, higher sampling rate and more precise resolution, the throughput of the PCI bus is the bottleneck for data readout. Moreover, to synchronize the system, an extra clock and trigger network should be designed to cooperate with the compact PCI based system.

In this paper, a new method to precisely digitize and read out data from the CSNS-WNS BaF_2 spectrometer is proposed. To capture the detector waveform precisely, a high-speed and large dynamic range digitizing technique with 1 GSps@12 bits is used, which can support good energy resolution of 1% at 662 keV. Furthermore, digitizing with a folding technique (not the traditional flash one) is used to lower the system power consumption.

To read out the massive data volume (peak rate up to 12 Gbps for each channel) generated from high precision digitizers in real time, a distributed architecture with 4 PXIe crates is designed, which can support excellent transfer bandwidth with several serial PCIe buses running in parallel. Data from the PXIe crates can be transmitted to the data acquisition system (DAQ) through 4 gigabit Ethernet cables in parallel.

To synchronize all the channels, a high precision clock and trigger distribution network is proposed, which can achieve good performance with jitter of about 12 ps (RMS). Critical signals can be distributed to the digitizers inside a crate through dedicated differential star paths, and to digitizers between crates through coaxial cable using signal conditioning and high speed serial communication.

Moreover, hardware-based trigger selection and zero compression algorithms are implemented in an FPGA to decrease the data rate.

2 Architecture of readout electronics

The readout electronics has a distributed architecture based on PXIe crates, as illustrated in Fig. 1. It mainly consists of the analog circuit, waveform digitizers, synchronous clock and trigger and data transmission network [10].

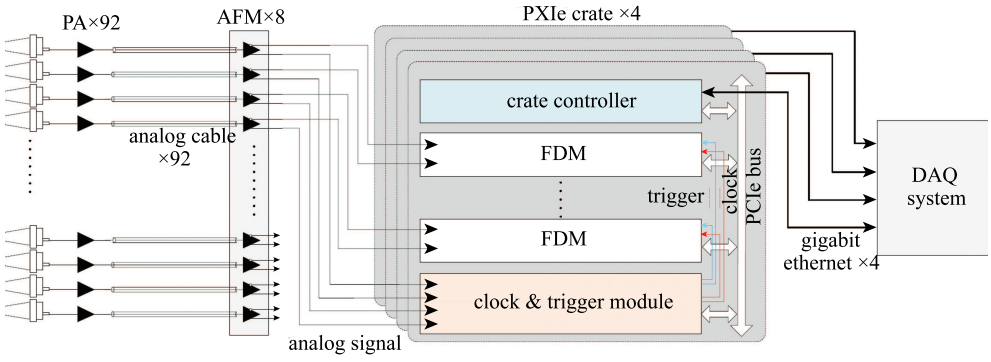

Fig. 1. Architecture of distributed readout electronics system.

The whole system contains 92 channels. The readout electronics system is located about 20 m away from the BaF_2 spectrometer, so a 20 m analog cable must be used to transmit the analog signal from the BaF_2 spectrometer to the readout electronics for each channel. A high bandwidth, high slew rate, low noise preamplifier is used to receive and adjust the analog signal at output of the detector. At the back end, each analog output is divided into two signals. One is sent to the digitizer, namely the field digitization module (FDM), for waveform digitizing, and the other is sent to the trigger module for trigger generation.

To achieve fast rise time and high SNR (signal-to-noise ratio), high bandwidth differential twisted-pair cable with shielding is adopted to transmit the analog signal. Correspondingly, the preamplifier is implemented with a fully differential amplifier to achieve single-ended to differential conversion. At the backend, a NIM based analog fan-out module (AFM) is designed to execute the signal deviation. The AFM is also implemented with a fully differential amplifier, which receives the differential signal from the cable and outputs a pair of differential voltage signals. The negative signal is sent to the FDM and the positive one is sent to the trigger module [9]. There are 8 AFMs in total and each AFM takes charge of 12 input channels. Because of the analog signal's wide frequency distribution, from nearly dc to 120 MHz, dc coupling is introduced along the whole transmission route.

To digitize up to 92 detector channels, there are 46 FDMs, each of which contains two digitizing channels. The FDMs are designed as standard PXIe 3U plugins and settled in 4 PXIe crates. Multi-channel, high-speed and high-resolution waveform digitizing leads to a huge data rate. To deal with the massive data readout and processing, a high-bandwidth PCIe bus and distributed structure with 4 PXIe crates are introduced into the readout electronics. Each crate contains a controller and several FDMs. To decrease the data rate, trigger selection and zero compression algorithms are implemented with hardware on the FDM. After being acquired in the FDM, the digitized signal is concentrated to the PXIe crate controller through the backplane PCIe bus and transmitted to the data acquisition system over gigabit Ethernet in parallel.

A high-precision synchronous clock and trigger network is designed to synchronize all the FDMs. To achieve high precision and a compact structure, the clock and trigger network is integrated with the backplane star buses of the PXIe crate. As all the star buses are concentrated on the system timing slot, we have to integrate the clock and trigger into one inseparable network.

The clock and trigger distribution network has a twin-stage structure. In the first stage, a global trigger and clock module (GTCM) produces and distributes clocks and triggers to local trigger and clock modules (LTCM) among the PXIe crates. In the second stage, LTCMs fan out triggers and clocks separately to other electronics plugins (mainly FDMs) inside the same crate, acting as buffers.

3 Waveform digitizer

A waveform digitizer called the field digitization module (FDM) is designed for acquiring the waveform of the detector signal. It is a crucial part of the readout electronics. As illustrated in Fig. 2, the FDM is designed as a standard PXIe 3U plugin. It is mainly composed of an ADC, a FPGA, two DDR3 memories, analog conditioning circuit, clock circuit, trigger circuit, PCIe and USB interface. The USB interface is spare for debugging [10].

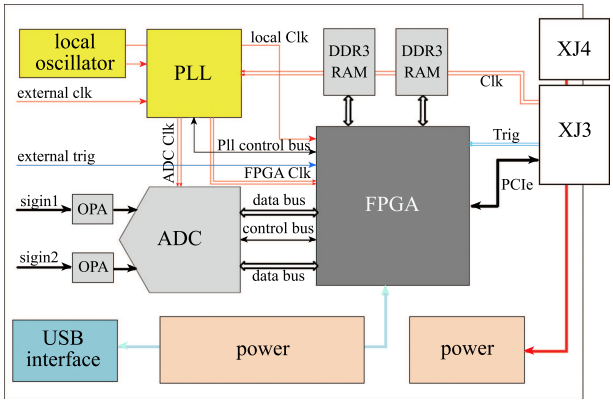

Fig. 2. Schematic of the field digitization module.

An ADC based on folding interpolation from TI (ADC12D1000) [11] is adopted to digitize the input signal on the FDM. It contains 2 channels, and each channel typically operates under a 1 GSps sampling rate with 12-bit resolution. It requires differential inputs and can provide 1.25 V common-mode voltage for dc-coupling. It is powered by a 1.9 V single supply and has a low power dissipation of about 1.7 W for each channel. To realize a dynamic range of up to 500 times and high-precision digitization, an ENOB (Effective Number of Bits) higher than 9 bits at about 100 MHz is required for the FDM.

To realize dc-coupling and accommodate the ADC input, a fully differential amplifier is used to buffer the analog input and achieve single-ended to differential conversion. A π-type resistor network is applied for terminating and attenuating the input signal. For further improving the SNR, an anti-aliasing filter is placed at the ADC input.

The clock for the FDM is buffered in from one of the PXIe's backplane differential star buses, PXIe_DstarA, which is driven in LVPECL signal with high performance (jitter lower than 3 ps and skew lower than 150

ps). A PLL (Phase Locked Loop) with jitter cleaner (LMK04821) [12] is used to multiply the clock frequency and filter out jitter noise, to achieve the high-precision 1 GHz sampling clock. Besides, a local oscillator is adopted for PLL configuration after power-up and an external clock interface is spare for debugging.

A high-performance Xilinx Kintex-7 series FPGA (XC7K160T-3FFG676) is adopted as the controller on the FDM. The FPGA takes charge of data receiving and processing in real time. For each channel, the FPGA receives the 12 Gbps data from the ADC, deserializes it into 96 bits at 125 MHz and caches in FIFO (First-In First-Out) memory. Once a valid trigger signal occurs, the effective data segment is selected and buffered into the next FIFO. After trigger selection, the zero compression algorithm is implemented for further decreasing the data rate. Finally, the data is packaged with trigger ID, buffered in DDR3 memories and sent to the PXIe crate controller by PCIe DMA. Two DDR3 memories operate in ping-pong mode, each of which has a capacity of up to 4 Gbits.

4 Clock and trigger network

A high-precision clock and trigger network is designed to synchronize the whole readout electronics. By analysis and simulation, to achieve an ENOB up to 9 bits and time resolution better than 1 ns, the 1 GHz sampling clock for the ADC should achieve high performance with jitter lower than 660 fs and skew far less than 1 ns. It requires the clock and trigger network to have a jitter lower than 100 ps and skew far less than 1 ns.

4.1 Clock and trigger generation

The clock frequency is 100 MHz, which is generated with a local oscillator on the GTCM (Global Trigger and Clock Module). A PLL (LMK04821) is used to filter out jitter noise and fan out the clock signal to internal logic and the GTX module of the FPGA. After being generated, the clock is distributed with high speed serial communication and clock data recovery (CDR) technique with the GTX module.

The trigger is generated by two steps, as shown in Fig. 3. For the first step, the STM (Sub Trigger Module) receives the analog signals and generates sub trigger information, which contains analog energy sum and over-threshold channels. The analog energy sum is achieved by analog integration and summation with operational amplifiers. It is sent to the GTCM with coaxial cable from the front panel. The over-threshold channel information is achieved by multi-channel discriminators and sent to the GTCM through PXIe_DstarC, a differential star bus from every peripheral slot to the system timing slot on the PXIe backplane. For the second step, the GTCM receives the sub trigger signals and generates the global trigger, according to the time window of the beam, multiplicity and energy threshold. There are 6 STMs, each of which takes charge of 16 analog inputs. The STMs are in the same PXIe crate as the GTCM.

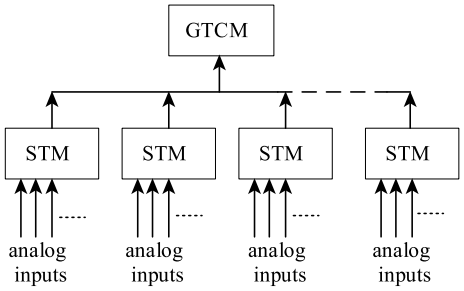

Fig. 3. Trigger generation network.

After being generated, the clock and trigger are distributed to every electronic channel through a common distribution network. The clock and trigger distribution network has a tree-like topology with a twin-stage structure, as shown in Fig. 4. The GTCM is responsible for generating the global trigger and clock, then distributing them to the LTCMs. An LTCM is responsible for fanning out clocks and triggers within the same crate. The GTCM is located at the system timing slot of the master PXIe crate while the three LTCMs are located at the system timing slots of the slave PXIe crates.

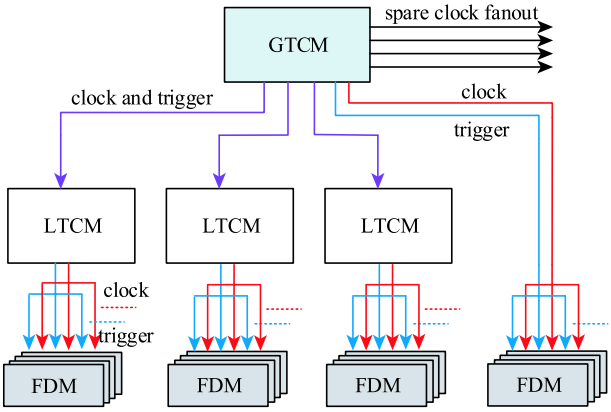

Fig. 4. Clock and trigger distribution network.

4.2 Clock and trigger distribution between crates

To achieve compactness and high precision, the clock and trigger distribution network are integrated with the backplane star fan-out buses of the PXIe crate. As all the star fan-out buses are concentrated on the system timing slot, the global clock and trigger distribution have to share one system timing slot plugin, the GTCM. This results in too many channels being integrated on the GTCM and too many cables being connected to the front panel of the GTCM, which conflicts with the limited area

of the front panel of the GTCM. To deal with this conflict, high speed serial communication and clock data recovery (CDR) technique are adopted to transmit the clock and trigger together.

Furthermore, single-ended transmission with coaxial cable is used to replace traditional differential transmission, to further simplify the distribution network, and micro-miniature coaxial (MMCX) connectors are used to save panel space. Pre-emphasis and equalization techniques are used to ensure the performance of the single-ended signal through a long coaxial cable. So, one coaxial cable can distribute the clock and trigger between crates at the same time. Modulation and demodulation of the clock and trigger are achieved by the GTX module in the FPGA. The baud rate on the coaxial cable is 1 GHz and the coaxial cable is about two meters long. The clock and trigger are recovered on the LTCM.

4.3 Clock and trigger fanning out inside a crate

A PXIe crate provides three sets of backplane star buses. PXIe_DstarA is a differential star fan-out bus driven by the LVPECL signal from the system timing slot to all peripheral slots. PXIe_DstarB is a differential star fan-out bus driven by the LVDS signal from the system timing slot to all peripheral slots. PXIe_DstarC is an oppositely directed star bus from every peripheral slot to the system timing slot. They can all achieve high performance with jitter lower than 3 ps and skew lower than 150 ps [13].

In this paper, PXIe_DstarA is used to fan out the clock, PXIe_DstarB is used to fan out the trigger and PXIe_DstarC is used to upload the sub-trigger information. By utilizing the backplane star buses, a high performance, highly concise clock and trigger network is achieved. Beside, a spare clock fan-out network is contained in the clock and trigger network for system expansion, as described in Ref. [14].

5 Tests and verification

Several tests were carried out to verify the key performance of the readout electronics, including the waveform digitizing test, the clock performance test, data transmission test and cosmic ray test.

5.1 Waveform digitizing performance

The waveform digitizing performance test was carried out with the FDM, and included a static performance test and dynamic performance test.

Sine waveforms with a frequency of 2.4 MHz were used for the static characteristics evaluation of the FDM. The static parameters were calculated with the code density method and ten million sampled points were used. Test results showed that the INL (Integral Non-Linearity) of the FDM ranged from −2.5 LSB (Least Significant Bit) to +1.5 LSB and the DNL (Differential Non-Linearity) ranged from −0.20 LSB to +0.20 LSB. The offset error was −0.99 LSB and the gain error was −0.02 LSB. Perfect static performance was achieved, which is similar to the parameters on the ADC's datasheet.

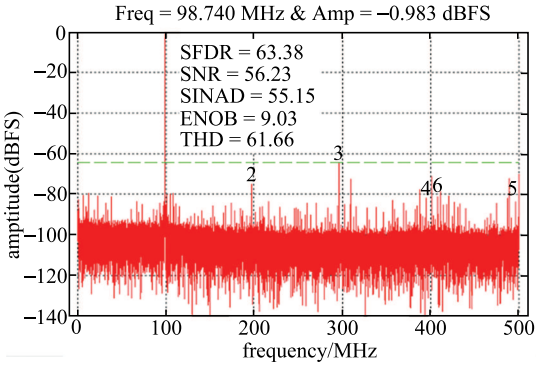

Fig. 5. Results of dynamic performance tests.

Sine waveforms with frequencies from 2.4 MHz to 198 MHz were used for the dynamic performance tests. Analysis was performed via FFT (Fast Fourier Transform) and 65536 sampled points were involved. Test results showed that the FDM achieved an ENOB above 9 bits with the frequency below 100 MHz, which indicates that dynamic range over 500 times and high energy resolution are achieved. The dynamic parameters at 98 MHz are illustrated in Fig. 5.

5.2 Data transmission capability

A block diagram of the data transmission network is shown in Fig. 6, with the transmission route covered from the FDM to the DAQ computer. A PCIe DMA was used to transmit data between the FDM and the crate controller, while gigabit Ethernet was used from the crate controller to the DAQ computer. The data transmission test was performed using a Linux operating system.

The test results show that an instantaneous data rate of 942 Mbit/s was achieved, which is more than 90% of the theoretical value. Four PXIe crates and four gigabit Ethernet cables running in parallel can meet the data transmission requirements of the BaF_2 spectrometer electronics.

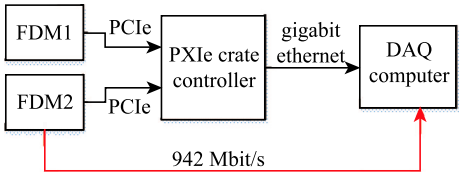

Fig. 6. Block diagram and result of data transmission test.

5.3 Clock performance

A clock performance test was performed to evaluate the clock performance after the clock and trigger network. The test block diagram is shown in Fig. 7. The GTCM and the test points on it were used to simulate the clock and trigger distribution network. The loop-back coaxial cable simulates the clock and trigger distribution process between crates. TP5 represents the terminal point of the clock transmission network.

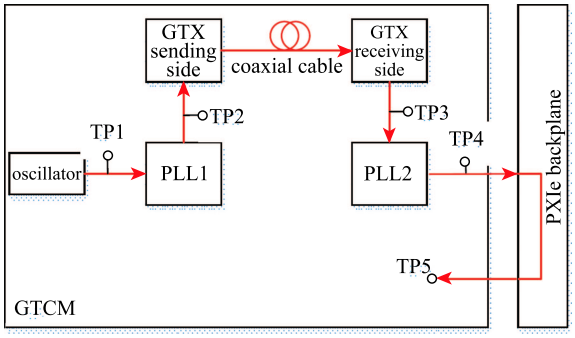

Fig. 7. Block diagram of clock performance test.

The clock jitter was measured by a Tektronix DPO5104 oscilloscope. It was characterized in TIE (Time Interval Error) at a population of 10^5, which is enough to get a highly accurate statistical result.

The test results are shown in Table 1. A low jitter of about 12 ps was achieved at the terminal point of the clock transmission network.

The skew of the clock was also obtained. As Fig. 8 shows, a low skew of about 200 ps was achieved between different slots within a PXIe crate.

Table 1. Jitter test results of the clock.

test point	TIE
TP1	17.2 ps
TP2	8.3 ps
TP3	0 m coaxial cable: 51.8 ps
	1 m coaxial cable: 49.7 ps
	2 m coaxial cable: 56.4 ps
	3 m coaxial cable: 61.2 ps
TP4	10.3 ps
TP5	12.2 ps

The clock performance test results show that a high performance with jitter of about 12 ps and skew of about 200 ps was achieved for the system clock. This meets the requirements of ENOB and time resolution for the electronics system.

5.4 Cosmic ray experiment

A cosmic ray experiment was carried out to evaluate the overall integration of the readout electronics system. The experiment platform contained a BaF_2 crystal, PMT and high-voltage module, preamplifier, AFM, FDM, PXIe crate and the data acquisition software, as illustrated in Fig. 9.

Typical waveforms of cosmic rays and alpha rays were acquired by the readout electronics system, as shown in Fig. 10 and Fig. 11, which indicates that the whole readout electronics system works well.

The cosmic ray waveform was precisely captured by the readout electronics. Obviously, the cosmic ray waveform has a fast component but the alpha ray does not.

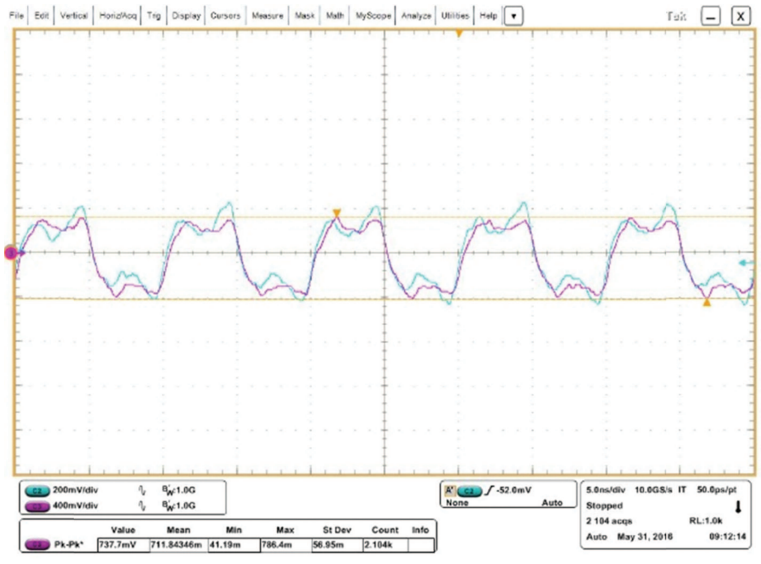

Fig. 8. Skew of the clock between different slots within a PXIe crate.

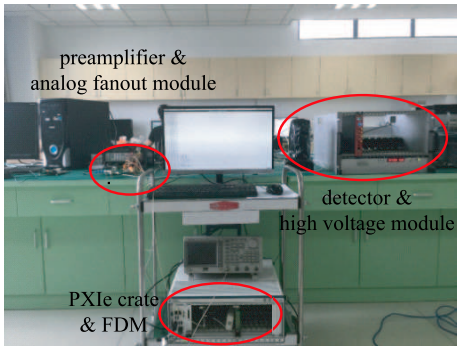

Fig. 9. (color online) The cosmic ray experiment platform.

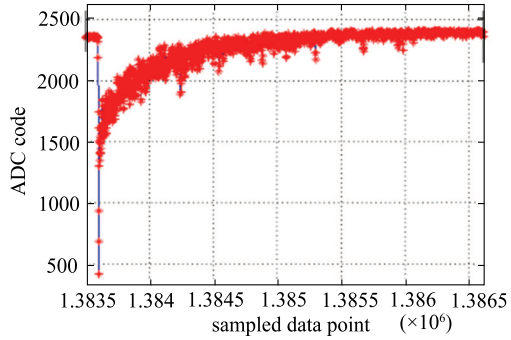

Fig. 10. Typical waveform for cosmic rays.

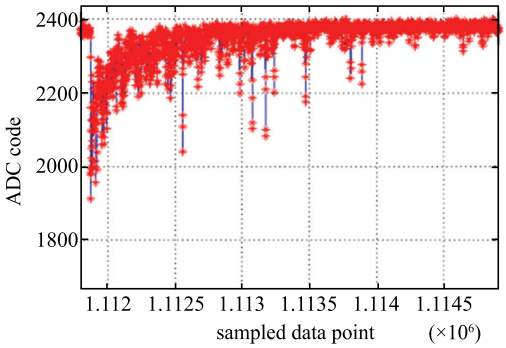

Fig. 11. Typical waveform for alpha rays.

Pulse shape discrimination methodology can be used to discriminate the γ-rays from the background alpha rays. Four sampling points were captured at the leading edge of the signal, which is similar to that captured by oscilloscope. Time of flight of the neutron can be obtained by a digital CFD algorithm, and the energy of the γ-ray can be calculated by numerical integration.

6 Conclusion

A new method for the BaF_2 spectrometer readout electronics is proposed. It has a distributed structure with 4 PXIe crates and 4 gigabit Ethernet cables. To precisely measure the (n, γ) cross section, a high speed, large dynamic range waveform digitizing technique with 1 GSps sampling rate and 12-bit resolution is used to precisely acquire the signal's waveform. A high-precision synchronous clock and trigger network based on PXIe is designed to synchronize all electronic channels.

The test results showed that the FDM achieved perfect static performance and dynamic performance. The data transmission network achieved a transmission rate of more than 90% of the theoretical value. The system clock achieved a high performance with jitter of about 12 ps and skew of about 200 ps. This performance meets the requirements of large dynamic range, high energy and time resolution, high data rate and low dead time for the BaF_2 spectrometer readout electronics. The whole readout electronics system worked well and cosmic ray waveforms were precisely captured.

The BaF_2 spectrometer readout electronics achieves high performance, compactness and high stability. It is extensible and upgradable in the future. This research can be used in other applications of high-energy physics experiments. The CSNS white neutron source project will be completed by the end of 2017 and the BaF_2 spectrometer readout electronics could provide a reference for other detectors in the CSNS-WNS project.

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