Design and performance of the LLRF system for CSNS/RCS *

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Abstract: The rapid cycling synchrotron (RCS) is part of the China Spallation Neutron Source (CSNS). The RCS provides 1.6 GeV protons with a repetition rate of 25 Hz. The RF system in RCS is mainly composed of a ferrite loaded RF cavity, a high power tetrode amplifier, a bias supply of 3300 A and a digital low level RF (LLRF) system based on FPGA. The major challenge of the LLRF system is to solve problems caused by rapid frequency sweeping and the heavy beam loading effect. A total of eight control loops are applied to ensure the normal operation. An effective feedforward scheme is widely used to improve the dynamic performance of the system. The design of the LLRF system and high power integration test results with the prototype RF system are presented.

Key words: LLRF, CSNS, RCS, RF

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1 Introduction

The China Spallation Neutron Source (CSNS) [1, 2] is composed of an H- linac and a proton rapid cycling synchrotron (RCS). It is designed to accelerate proton beam pulses to 1.6 GeV, striking a metal target to produce a spallation neutron for scientific research. The injection and extraction beam energy in CSNS/RCS are 80 MeV and 1.6 GeV respectively. Table 1 summarizes the primary parameters related to the RF system.

Table 1. RF system parameters for CSNS/RCS.

parameters	value
beam power/kW	100
circumference/m	229.7
energy/GeV	0.081–1.6
intensity (ppp)	1.87E13
circulating dc current/A	1.5/3.6
repetition rate/Hz	25
harmonic number	2
RF frequency/MHz	1.02–2.44
peak RF voltage/kV	165 (h=2)

A total of 8 fundamental RF systems are used in CSNS/RCS to provide a peak RF voltage of 165 kV. The RF systems operate on the harmonic number h=2, and the frequency sweeps from 1.022 MHz at injection to 2.444 MHz at extraction with a repetition rate of 25 Hz. Fig. 1 shows the frequency, amplitude and synchronous phase patterns during an accelerating time of 20 ms. According to the working pattern, the frequency, the amplitude and the phase of the RF signal should be carefully controlled. The CSNS/RCS LLRF control system is designed to achieve required acceleration voltage amplitude and phase regulation of ±1% and ±1° respectively. The resonant state of the cavity and the high beam loading effect should also be taken care of by the low level RF (LLRF) system, to ensure the stability of the RF system.

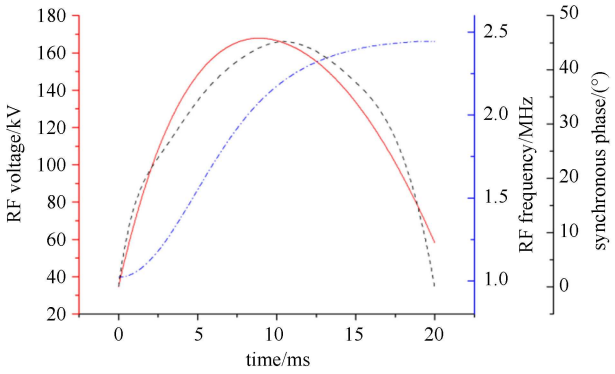

Fig. 1. (color online) RF frequency (dot-dash line) accelerating voltage (solid line) and synchronous phase (dot line).

2 CSNS/RCS RF system

In CSNS/RCS, each RF is mainly composed of a cavity, a bias supply, a high power RF amplifier and a digital LLRF system [3]. The cavity used is a ferrite-loaded coaxial resonator with two accelerating gaps and is single

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ended. The loaded material is Ferroxcube 4M2. The inductance of the cavity can be shifted as a bias field alteration. Corresponding to the bias current varying range of 200–3000 A, the resonant frequency of the cavity can sweep from 1.02 to 2.44 MHz to satisfy the CSNS/RCS operation. For one gap, a nominal peak RF gap voltage of more than 11.8 kV is required. In order to satisfy the requirement of cavity dynamic tuning caused by the nonlinear characteristics of the ferrite material during rapid sweeping of the RF frequency and voltage, a 3300 A switch type power supply and a 150 A linear type power supply are used in the bias supply. Two types of power supply are connected in parallel, and a big range more than 3000 A and a high bandwidth up to 20 kHz can be achieved respectively. The RF amplifier consists of a three stage amplifiers chain. The final stage amplifier uses a tetrode TH558 operated in class AB1, with a cathode-grounded configuration. The maximum plate dissipation of the tube is 500 kW. The tetrode is driven by a feedback (FB) amplifier of 800 W located in the rack of the final stage amplifier adjacent to the cavity. The RF drive signal from a wide-band solid-state preamplifier of 500 W will be combined with an RF signal extracted from the cavity which has a proper amplitude and delay to drive the FB amplifier. Fig. 2 shows the simplified schematic of the CSNS/RCS RF system.

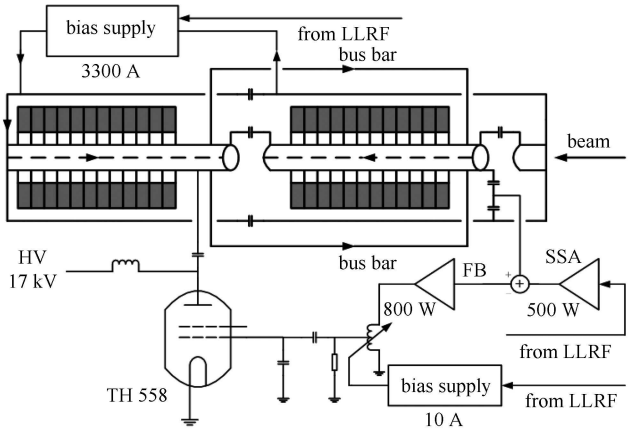

Fig. 2. CSNS/RCS RF system simplified schematic.

3 LLRF system overview [4]

Considering the system compatibility and bandwidth, a CPCI bus is adopted. The hardware platform includes the CPCI6200 CPU, the CSNS standard timing board to receive a system clock and event trigger, the custom CPCI carrier to realize RF signal digitization data processing and control arithmetic for control function. The hardware is arranged into two CPCI chassis. One is for acceleration voltage control and cavity dynamic tuning. Another is for beam orbit correction and beam loading compensation.

The custom CPCI carrier is the heart of the LLRF control system. It features one Stratix IV EP4SGX530 FPGA which provides 531.2 K equivalent logic elements. It also includes high performance TMS320C6655 DSP, PCI9656 CPCI bridge chip, high speed ADC and DAC with a sampling rate up to 125 MHz, optical interface, ethernet interface, and so on. Operation command and control data exchange protocol between the CPCI6200 and the CPCI carriers were carefully defined. The custom driver was developed to access specified registers on CPCI carriers from CPCI6200 running the VxWorks operating system. Adhering to the CSNS control standard, the LLRF control system is Experimental Physics and Industrial Control System (EPICS)-based. EPICS drivers have been developed to provide user interface through standard Channel Access protocol. As shown in Fig. 3, each custom CPCI carrier has an allocated time slot of 2.25 ms for transmission data in 25 Hz system operation and the actual bandwidth is greater than 200 MB/s. A self-defined bus based on LVDS is adopted to transmit control data, which is shared by the CPCI carriers. The event trigger and following clock are used to ensure the reliability and stability of transmission, and

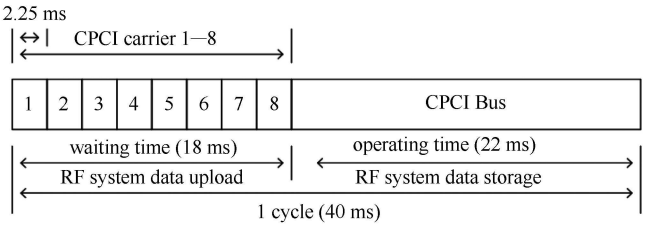

Fig. 3. CPCI bus operation timing.

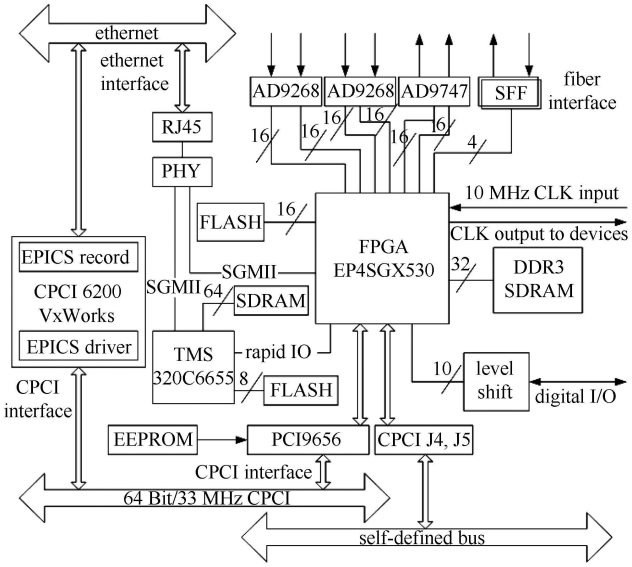

Fig. 4. LLRF system configuration.

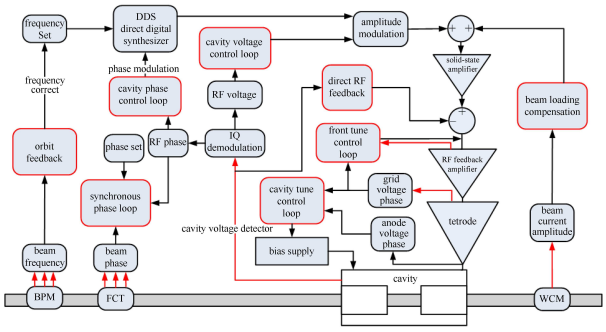

Fig. 5. (color online)Block diagram of the LLRF control system.

the maximum bandwidth is greater than 3.84 Gb/s. Fig. 4 shows the configuration of the LLRF control system.

4 Control architecture of the LLRF system

Each RF system has an independent LLRF system based on FPGA which is composed of eight control loops including a cavity voltage loop, cavity phase loop, synchronous phase loop, cavity tune loop, tetrode grid tune loop, beam loading compensation loop, orbit feedback loop, and direct RF feedback loop [5, 6]. Fig. 5 shows the block diagram of the LLRF control system.

4.1 RF signal processing

For most control loops in a CSNS/RCS LLRF control system, the procedure of signal processing works in much the same way. The RF and reference signal are both generated by a Direct Digital Synthesizer module. To satisfy the sweeping frequency work status of the RF system, a direct demodulation method is adopted in the LLRF system. All RF signals are sampled with 40 MHz, and then digital signals are separately multiplied by two reference signals for orthogonal demodulation. A 70 taps FIR low-pass filter is adopted with 1.75 μs delay. The Coordinate Rotation Digital Computer algorithm is also used to compute trigonometric functions and obtain the amplitude and phase of the signals. Fig. 6 shows the procedure of signal processing.

4.2 Feedforward compensation

A simple and effective feedforward scheme is explored and applied in the CSNS/RCS LLRF control system. The input and output data of the control module in one cycle are stored respectively. An overall average of last N cycles data is calculated to eliminate the impact of random error, where N is the quantity of stored data, and its value decides the sensitivity of the feedforward scheme. A coefficient based on the transfer function will be multiplied by the averaged input data, and then added to the averaged output data to generate the feedforward pattern.

In the future, a frequency filter method will be used in the feedforward scheme to avoid system oscillation. Through fast Fourier transform of the input and output data, only the component below the bandwidth of the control module will be stored.

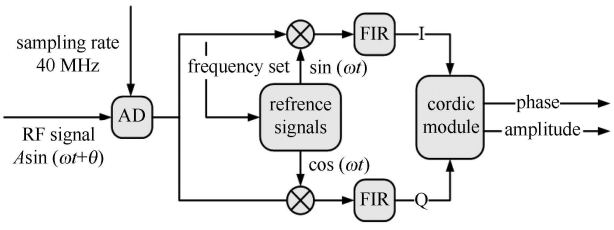

Fig. 6. Procedure of signal processing.

4.3 Cavity voltage loop

The cavity voltage loop exists individually for each cavity at (h=2), and makes the cavity voltage follow a pattern shown in Fig. 1. Each cavity has two acceleration gaps in parallel. For one gap, the minimum voltage is 1.3 kV and the maximum voltage is 10.3 kV.

A feedforward compensation scheme (as shown in the previous section) is used to decrease the following error induced by the rapid change of cavity voltage.

4.4 Cavity phase loop

The cavity phase loop locks the phase between the accelerating voltage and the RF reference signal. The initial phase of the RF reference signal is triggered by the timing system, when the beam is injected into the RCS. The cavity phase loop should compensate the phase shift mainly caused by two stages of tune loops and frequency response in the amplification chains. The bandwidth of the cavity phase loop should be much higher than the tune loops to avoid loops coupling. When detuning happens, the cavity phase loop must immediately adjust the phase of the RF driving signal to maintain the correct phase of the accelerating voltage.

4.5 Synchronous phase loop

The synchronous phase loop damps synchrotron oscillation. The beam phase is detected by the Fast Current Transformer, and compared with the phase of the accelerating voltage. According to the result of comparison, the synchronous phase loop provides a damping component with a 90 degree phase shift into the RF diver signal.

4.6 Cavity tune loop

The cavity tune loop is fed by the phase between the grid voltage of the tetrode and the cavity voltage. The change of resonant frequency of the cavity from 1.22 to 2.444 MHz corresponds to the bias current changing from

about 200 to 3000 A.

Due to the bandwidth limitation of the bias supply, a similar feedforward compensation scheme is used for the 25 Hz system operation.

4.7 Tetrode grid tune loop

The tetrode grid tune loop is used to compensate the parasitic capacitance of the tetrode grid, and ensure system gain and stability in operating frequency range. A linear bias supply of 12 A is used to change the inductance of a ferrite-loaded low-Q resonant circuit, as shown in Fig. 2. There is only a feedback loop for the tetrode grid tuning. Except for this, both of the tetrode grid tune loop and the cavity tune loop have the same operating principle.

4.8 Beam loading compensation loop

The circulating current in CSNS/RCS is fairly high, and the beam loading effect must be carefully considered. A classic feedforward algorithm is adopted for the beam loading compensation. The beam signal is picked up by a wall current monitor, and added into the RF drive signal with an opposite phase. The fundamental component of the beam signal is taken out, and given the proper gain and phase [7].

Because of the two stages of tuning loops, some phase error will be introduced. An adaptive algorithm is now being developed for adjusting the phase setting of the feedforward algorithm.

4.9 Orbit feedback loop

The orbit feedback loop is reserved to adjust the initial frequency setting. The beam signal is picked up by a beam position monitor, and used to compute the modification value.

4.10 Direct RF feedback loop

The RF feedback is an analog control loop. On account of the characteristics of low latency and high bandwidth, it is adopted to reduce transient beam loading and enhance the dynamic performance of the LLRF system. A small fraction of cavity voltage is picked up and fed back to the feedback amplifier. The phase shift in the feedback path is guaranteed by the two stages of tuning loops. Since there are no filters and signal demodulation, the RF feedback loop responses any disturbance of arbitrary frequency. In practice, the feedback gain is about 20 db.

5 System testing results

The R&D prototype of the RCS RF system has been developed, including a full size ferrite-loaded RF cavity, a set of RF amplifiers, a 3300 A bias supply and a digital LLRF system, as shown in Fig. 7.

The high power integration test was completed on the prototype of the RF system, with the cavity voltage loop, cavity phase loop, cavity tuning loop, tetrode grid tuning loop, and RF feedback loop. Except for the beam related control loops, the entire LLRF system is verified by the integration test. The maximum cavity voltage up to 12 kV is achieved, with the RF frequency sweeping from 1.022 to 2.444 MHz and a repetition rate of 25 Hz. The working time of the RF system in one cycle is 22 ms. The first 2 ms is preparation time to initialize the tuning state and establish a stable cavity voltage with proper amplitude and phase. The following 20 ms is the acceleration time, and the RF system runs in accordance with the working pattern. The waveform of the cavity voltage and grid voltage of the tetrode are shown in Fig. 8.

Fig. 7. View of the CSNS/RCS RF system prototypes.

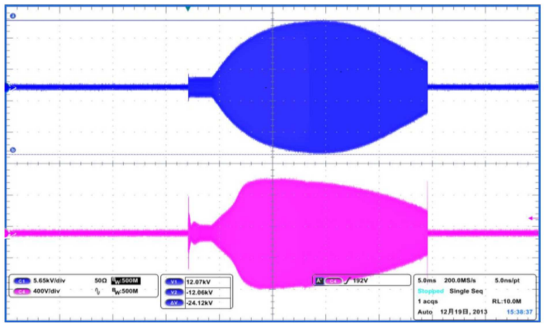

Fig. 8. (color online)Waveform of the cavity voltage (above) and grid voltage of the tetrode(below) on oscilloscope.

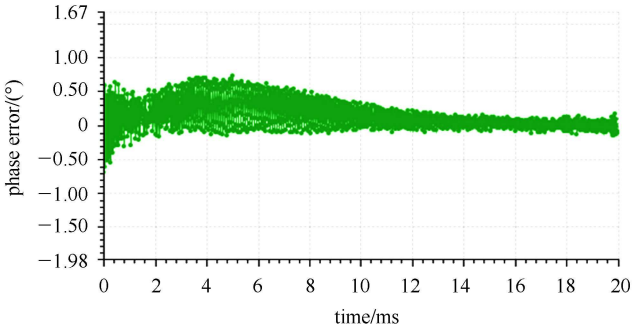

Fig. 9. (color online)Cavity phase error in one cycle.

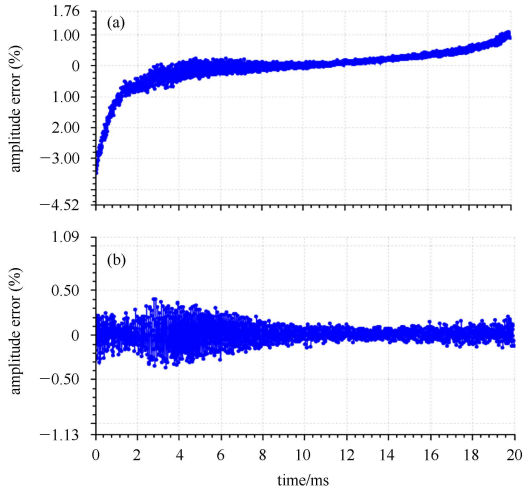

Fig. 10. (color online) Cavity voltage error in one cycle without (a) and with (b) feedforward compensation.

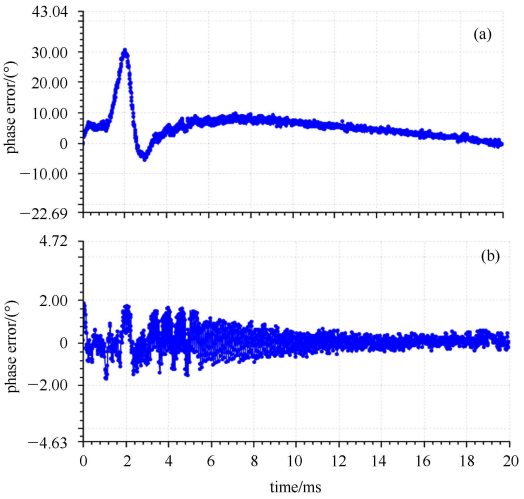

Fig. 11. (color online) Cavity tuning error in one cycle without (a) and with (b) feedforward compensation.

Figure 9 shows the phase error between the cavity voltage and the RF reference signal. With the cavity phase loop, the phase shift introduced by amplification chains including 2 stages of tune loops, decrease to ±0.6 degree.

As shown in Fig. 10, due to the dynamic range of the cavity voltage, the amplitude error is more than 3% at the beginning of one cycle with only feedback control, and decreases to less than ±0.4% with the feedforward compensation.

The algorithm of feedforward compensation used in the cavity tune loop is similar to the cavity voltage loop. The maximum cavity tune error decreases from about 30° to 2°, as shown in Fig. 11.

Because the Q value of the resonant circuit is much smaller than the cavity, the bandwidth of the grid tune is higher than the cavity. Therefore, there is only a feedback control adopted. As shown in Fig. 12, the maximum grid tune error is about 1.3°.

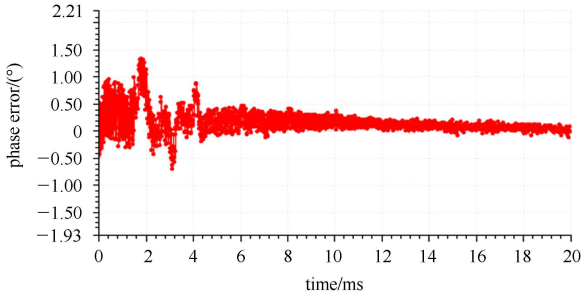

Fig. 12. (color online) Grid tuning error in one cycle.

6 Summary

The CSNS/RCS LLRF system provides a total solution for the RF system in RCS with rapid frequency sweeping and the heavy beam loading effect. The cavity tuning and beam loading compensation are the key issues, and need to be properly handled. Feedforward compensation is widely used to improve dynamic performance and stability of the system. The bandwidth of different control loops should be carefully set to avoid coupling oscillation.

References

1 WANG Sheng et al. Chin. Phys. C, 2009, **33**(Suppl. II): 1–3
2 WEI J et al. Nucl. Instrum. Methods A, 2009, **600**: 10–13
3 SUN Hong et al. IPAC, 2013. 2765–2767
4 LI Xiao et al. IPAC, 2013. 2977–2979
5 LI Xiao. Study on the Digital Low Level RF Control System of CSNS/RCS (PhD Thesis). Beijing: Graduate University of Chinese Academy of Sciences, 2010 (in Chinese)
6 Tamura F et al. PAC, 2005. 3624–3626
7 LI Xiao et al. High Power Laser and Particle Beams, 2013, **25**(10): 2671–2674 (in Chinese)