Study of the dose rate effect of 180 nm nMOSFETs *

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Abstract: Radiation induced offstate leakage in the shallow trench isolation regions of SIMC 0.18 μm nMOSFETs is studied as a function of dose rate. A "true" dose rate effect (TDRE) is observed. Increased damage is observed at low dose rate (LDR) than at high dose rate (HDR) when annealing is taken into account. A new method of simulating radiation induced degradation in shallow trench isolation (STI) is presented. A comparison of radiation induced offstate leakage current in test nMOSFETs between total dose irradiation experiments and simulation results exhibits excellent agreement. The investigation results imply that the enhancement of the leakage current may be worse for the dose rate encountered in the environment of space.

Key words: dose rate effect, MOSFET, ELDRS, total dose

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1 Introduction

The increased damage at low dose rate that occurs in bipolar linear devices has been widely studied, as summarized in Ref. [1]. It is related to the thick oxides and very low electric fields, resulting in long hole transport times. There has been very little work done to investigate the enhanced low dose rate sensitivity (ELDRS) effects in CMOS [2–5]. At present, the ELDRS effects in devices of MOS technologies have remained a very controversial point due to the lack of sufficient experimental information. Shallow trench isolation (STI) structures are considered as the main remaining total dose problem in scaled CMOS devices [6]. The STI used to isolate transistors still has a thickness of several 100 nm. Therefore, this oxide is expected to be very sensitive to radiation. The charge trapping in the sidewall of trench oxides results in excessive leakage by inverting the channel of the parasitic transistors in NMOS transistors [7, 8]. In addition, the electric fields from trench oxides are far lower than those within gate oxides. The dose rate sensitivity as applied to radiation induced edge leakage in SMIC 0.18 μm nMOSFETs is examined in this paper.

2 Experimental approaches

The radiation samples used in this work are drawn from SMIC 0.18 μm process nMOSFETs. Two types of transistors (i.e., W/L=0.5/0.18 and 5/0.18) were chosen. All irradiations were performed in ^{60}Co sources at the Northwest Institute of Nuclear Technology. Dose rates of 0.5 rad (Si)/s and 50 rad (Si)/s were chosen. The test devices were irradiated under bias with 1.8 V on the gate and all of the other terminals were grounded. The samples were removed from the ^{60}Co sources for electrical measurement and I-V curves were collected with a computer controlled HP4156A precision semiconductor parameter analyzer. A 25° anneal test after high dose rate irradiation was performed under the same bias.

3 Experimental results

3.1 Total dose dependence

Figure 1 shows the I-V curves for 0.18 μm process nMOSFETs before and after irradiation. Significant offstate leakage current increase is observed. A lack of parallel shift of the I-V characteristics along the X-axis (gate bias) with dose indicates negligible buildup of oxide-trapped charge or interface traps in the thin gate oxide [9].

Since the radiation induced threshold voltage shift has essentially vanished, this leaves field oxide isolation structures as the main remaining total dose problem. A gate bias of 0 V corresponds to the offstate operation of the transistor. Radiation induced charge buildup in the field oxide causes the offstate leakage current to increase sharply. It is this current which is the focus of this work.

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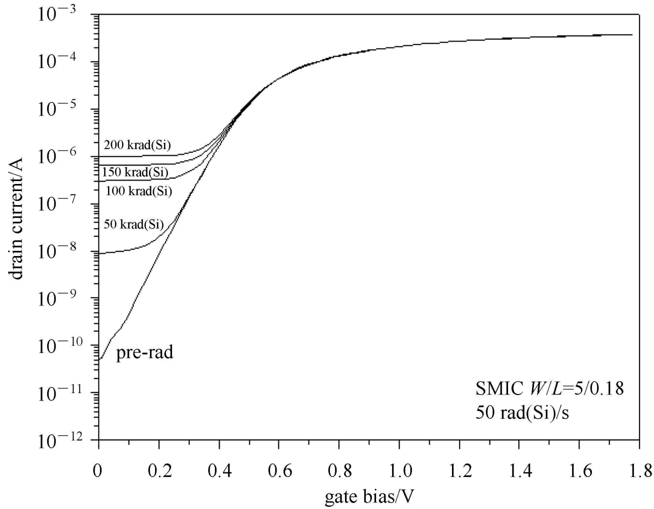

Fig. 1. Dependence of sub-threshold current characteristics on total dose for the 0.18 μm nMOSFETs. The I-V characteristics were measured at $V_{\rm D}$=0.05 V.

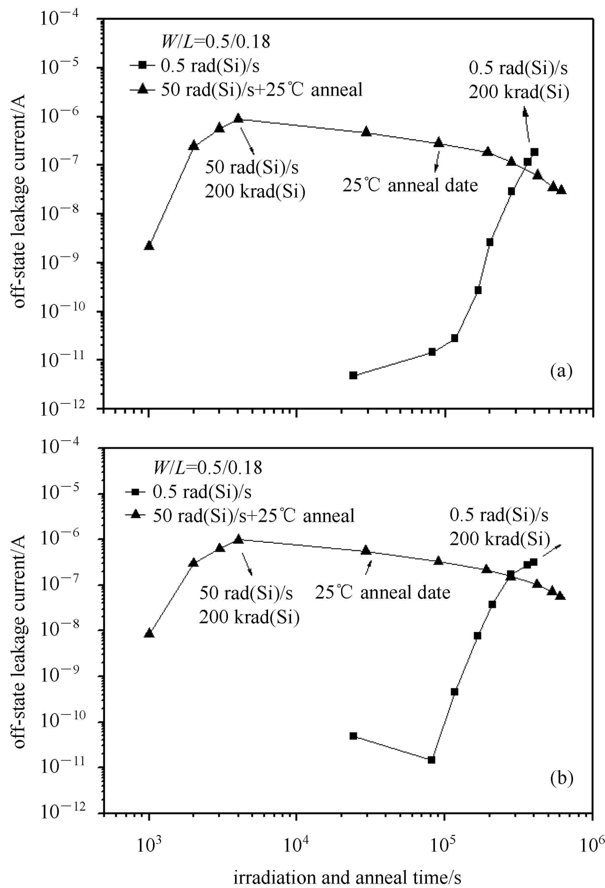

Fig. 2. Experimental result of dose rate dependence of off-state leakage current for the SMIC 0.18 μm nMOSFETs.

3.2 Dose rate dependence

The dependence of radiation induced offstate leakage current on dose rate was examined. Test nMOSFETs from the SMIC 0.18 μm process were irradiated at two dose rates(0.5 rad(Si)/s and 50 rad(Si)/s) and they accumulated a total ionizing dose of up to 200 krad(Si). Following high dose rate (HDR) exposure, devices were annealed at room temperature with the same biasing configuration. The offstate leakage current from two size transistor are shown as a function of irradiation and annealing time in Fig. 2(a) and (b). At the same total dose, degradation is more severe at a low dose rate (LDR) exposure than a high dose rate exposure with the corresponding room temperature anneal. The results indicate that there is a LDR to HDR enhancement factor (EF) of approximately 2.8 for Fig. 2(a) and approximately 2.5 for Fig. 2(b). This phenomenon from SMIC 0.18 μm devices was regarded as a "true" dose rate effect (TDRE) and not as a time dependent effect (TDE) [10]. A "true" low dose rate effect means that the degradation at the end of LDR irradiation is greater than the degradation measured after irradiation to the same dose at HDR followed by a room temperature anneal for a time at least as long as the irradiation time at LDR.

This experimental result suggests that the enhancement in leakage current may be worst for the dose rate encountered in the environment of space. The HDR irradiation with the corresponding room temperature anneals will underestimate the effect of LDR irradiation.

4 Physical model

The edge-leakage current for the SMIC 0.18 μm device results from the competing effects of charge buildup during irradiation and annealing of the charge during and after irradiation [11]. To account for the time dependencies of these processes, we employed a simple model for holes trapping and detrapping in the field oxide to analyze charge transport and trapping, and provide additional insight into the mechanisms for the dose rate sensitivity of the SIMC 0.18 μm nMOSFETs

The annealing rate of a trapped hole depends exponentially on the distance of the trap from the interface [10]. To account for variations in anneal time with trap position, x, multiple position were assured for a single trap energy. During irradiation, the trapped hole density, $p_{\rm t}$ at a given position was modeled with [12]

$$\frac{{\rm d}p_{\rm t}}{{\rm d}t}=gk_1(N_{\rm t}-p_{\rm t})-k_2p_{\rm t}, \tag{1}$$

where g is the dose rate, $N_{\rm t}$ is the hole trap density, k_1 and k_2 are rate constants for the hole trapping and annealing, respectively. This equation states that the rate of charge buildup is determined by the relative rate of

hole trapping and annealing. Assuming the initial condition $p_t(0)=0$, the trapped hole density during irradiation was given by:

$$p_t(t)=\frac{gk_1N_t}{gk_1+k_2}\cdot\left(1-e^{-(gk_1+k_2)t}\right). \quad (2)$$

The trapped hole density during postirradiation annealing was obtained by solving (1) with $g=0$ to give:

$$p_t(t)=p_t(t_r)\cdot e^{-k_2(t-t_r)}. \quad (3)$$

Where the density immediately followed irradiation, $p_t(t_r)$, is obtained from (2) for the appropriate dose rate and irradiation time.

The dominant charge loss mechanism for irradiation MOS devices at room temperature is direct tunneling of holes out of the oxide into the silicon substrate. Assuming that the probability of a hole tunneling from the oxide depends exponentially on the distance from the trap to the Si/SiO_2 interface [13], and is given by:

$$k_2=\alpha\cdot e^{-\beta\cdot x}, \quad (4)$$

where α is the attempt to escape frequency β is related to the tunneling barrier. So, the trapped hole density during post-irradiation annealing is given by

$$p_t(t)=p_t(t_r)\cdot e^{-\alpha\cdot e^{-\beta\cdot x}(t-t_r)}, \quad (5)$$

where $p_t(t_r)$ is the distribution of trapped holes immediately following irradiation. The annealing effects of post-irradiation for MOS oxide can be obtained by using (5).

5 Method of simulation

5.1 Model parameters validation

The trapped hole density was related to offstate leakage current for transistors from the SIMC 0.18 μm process using ISE-TCAD software. SA schematic view of simulated structure of shallow trench isolation on the SMIC 0.18 μm nMOSFET is shown in Fig. 3, along with the drain to source inversion leakage path that we are considering in this study. Although other leakage paths are possible, we will consider only the lateral leakage path from drain to source, which is produced by trapped holes along the interface between the p-well and the shallow trench isolation that surrounds the nMOS transistor.

Charge trapping in the field oxide was simulated by placing a uniform density of positive charge along the interface between the Si and the field oxide. Six evenly spaced trap positions over a range of ∼5 nm were used in the model, where the trap density at each position was assumed to be $N_t=2\times10^{17}cm^{-3}$. A comparison of model to experimental data was accomplished by fitting parameters k_1 and k_2 to match the simulated leakage currents to the measured leakage currents. The values for the rate constants were chosen to match the simulated and experimental data at highest dose rate: $k_1=1.15\times10^{-5}$ rad(Si)$^{-1}$, $\alpha=4.9\times10^{-5}$ cm^{-1}, and $\beta=0.95$ nm^{-1}

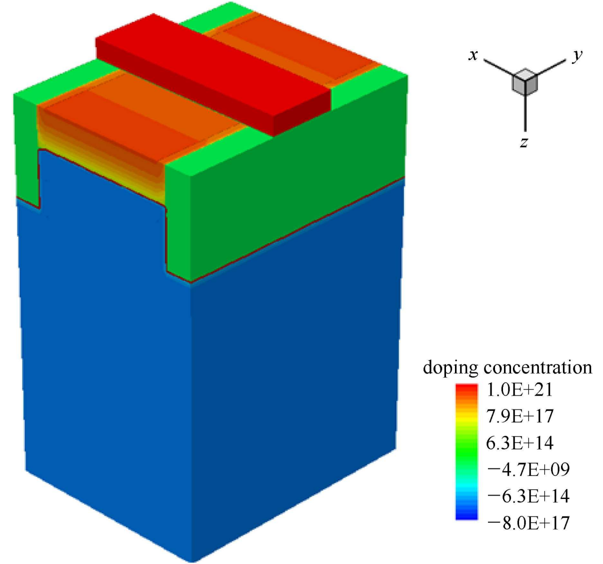

Fig. 3. (color online) A schematic view of simulated structure of shallow trench isolation on the SMIC 0.18 μm nMOSFETs.

5.2 Hump effects

Figure 4 shows the total dose simulation result of 0.18 μm process nMOSFETs before and after irradiation. A sub-threshold hump effect after irradiation at a dose level below 200 krad(Si) is observed by placing a uniform density of positive charge over the entire STI sidewall. Significant sub-threshold humps appear, even for a relatively low total dose. Instead of applying a

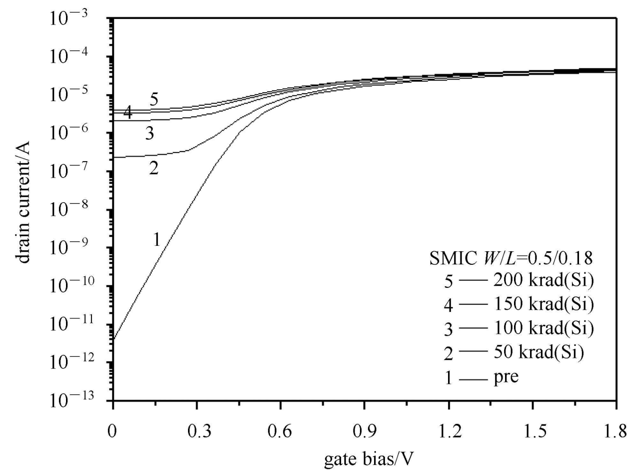

Fig. 4. *I-V* curves for the 0.18 μm nMOSFETs simulated with the 3-D model by placing a uniform density of positive charge over the entire trench wall.

uniform charge density all along the trench sidewall, we used a charge distribution in which the upper region of the trench sidewall contains little or no trapped charge. The hump effect disappeared when a uniform density of positive charge was placed 100 nm under the trench oxide from the STI corner (Fig. 5). Our simulation result shows that the charge trapped at the STI corner is the major reason for the hump effect. From Fig. 5 it can be seen that the 3-D simulations resulted in leakage characteristics that are very similar to the measured data. The reason is considered to be due to the charges inside the STI oxide being pushed down by the vertical electric field coming from the positive gate bias, leaving much less total dose induced charge close to the top of trench.

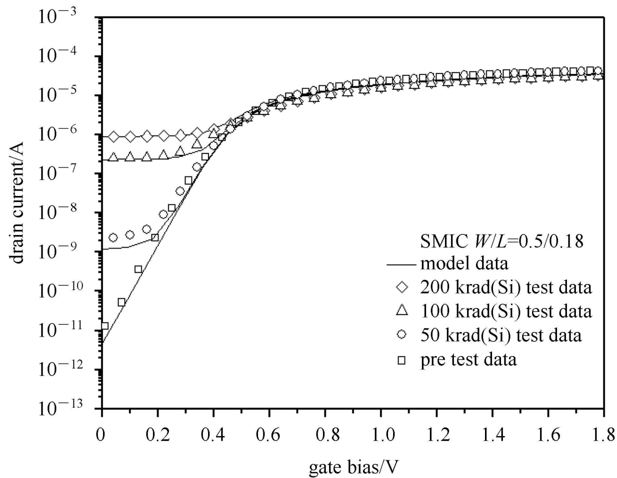

Fig. 5. *I-V* curves for 0.18 μm nMOSFETs simulated with the 3-D model by placing a uniform density of positive charge under 100nm the trench oxide from the STI corner.

5.3 Mechanism for dose rate sensitivity

Our analysis of the example given in Fig. 2(a) and (b) shows that, because the anneal time for trapped holes during low dose rate irradiation is longer, the offstate leakage current at LDR irradiation is smaller than that due to only HDR irradiation. However, for a long anneal time, the degradation becomes sensitive to dose rate, the holes trapped at low dose rate and high dose rate have a comparable time to the anneal, and the offstate leakage current at LDR irradiation is greater than that due to HDR irradiation and anneal. These experimental results imply that the anneal rate must increase with dose rate, which is consistent with the idea that decreasing the dose rate causes holes to be trapped further from the Si-SiO_2 interface. That is to say, the range position of charge trapping moves away from the interface at LDR irradiation. So, the shift of trap occupancy was modeled with $k_2=\alpha\exp(-\beta(x+x_0))$ in the ISE-TCAD simulation, where $x_0=0.6$ nm for LDR irradiation. Fig. 6 shows the simulated off-state leakage current at two dose rates of irradiation after a total dose radiation level of 200 krad(Si) for W/L=0.5/0.18 NMOS transistor versus anneal time. Fig. 6 shows that, at the same time, the offstate leakage current at LDR is greater than HDR. The simulation result is consistent with the experimental data in Fig. 2(a) The nMOSFETs transistors from SMIC 0.18 μm process indicate a “true” dose rate effect.

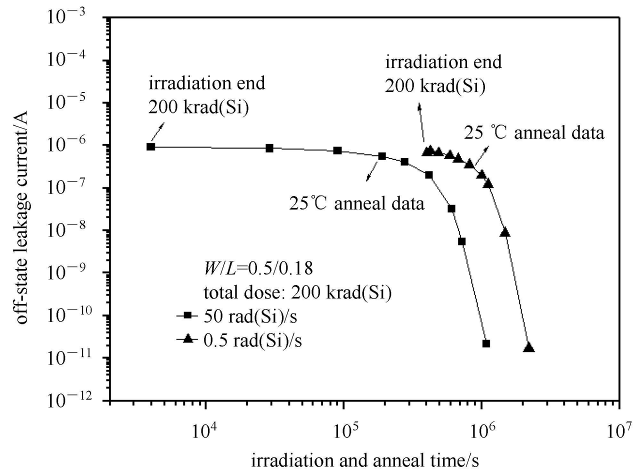

Fig. 6. Simulation result of dose rate dependence of off-state leakage current for the SMIC 0.18 μm nMOSFETs.

Dose rate sensitivity can result from the space charge in the field oxide. Space charge is thought to affect charge transport, altering the region where charge is collected at the interface, and the trapped positive charge is closer to the interface at a high dose rate [2] because tunneling time constants for holes increase exponentially with distance from the interface [13]. A small shift in the trapped hole distribution towards the interface may increase the annealing rate following high dose rate irradiation. So the annealing rate of high dose rate is faster than low dose rate.

6 Hardness assurance implications

The MIL-STD-883H method 1019.8 defines a test procedure used by the defense industry to assess the ionizing radiation hardness of packaged MOS devices at a low dose rate environment, such as space [14]. The test procedure includes separate test sequences for the effects of radiation induced oxide trapped charge and interface traps on device performance. As shown in Fig. 7, the main flow of this test consists of two parts. Part Ⅰ of the method is a conservative test for parametric or functional failure due to radiation induced oxide trapped charge. Part Ⅱ of the method is a conservative test for parametric or functional failure due to long term buildup of interface traps.

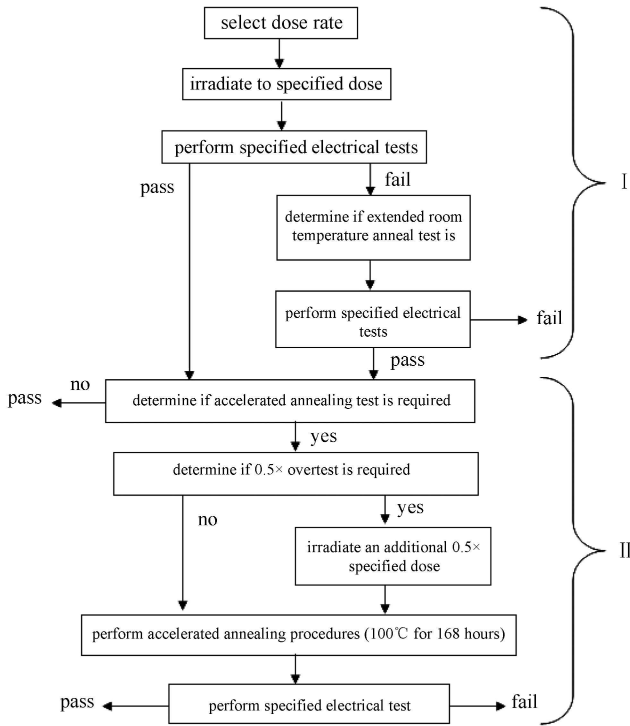

Fig. 7. Flow diagram of the ionizing radiation test procedure for MOS devices.

The results from our investigation show that the response from HDR irradiation with the corresponding room temperature anneals is smaller than that from LDR irradiation. Such an extended room temperature anneal test in Part Ⅰ will not bound the low dose rate response for the SMIC 0.18 μm test devices. The results from HDR irradiation with the corresponding room temperature anneals will underestimate the effect of LDR irradiation. So, one means to provide a more accurate estimate of LDR irradiation is to deal with the dose rate dependence by applying an enhancing factor to the high dose rate data. Another way is to run the irradiation tests in a low dose rate irradiation environment.

7 Conclusion

The irradiation and anneal responses of SIMC 0.18 μm nMOSFETs have been examined. A significant difference was observed in CMOS devices with trench isolation when they are irradiated at a low dose rate compared to the results at a high dose rate. Offstate leakage current was found to increase with decreasing dose rate when annealing is taken into account. The nMOSFETs from the SMIC 0.18 μm CMOS process exhibit ELDRS effects. This phenomenon can be regarded as a “true” dose rate effect. A physical model and new method of simulation radiation induced degradation in STI are presented. Comparison of radiation induced leakage current in test nMOSFETs between irradiation experiments and simulation results exhibits excellent agreement. The investigation results in this paper suggest that extended room-temperature anneal tests, such as those prescribed by MIL-STD-883H Method 1019.8, may not be conservative enough for the hardness assurance testing of some advanced CMOS devices. This needs to be considered for the new testing and hardness assurance of advanced CMOS, where STI leakage is the dominant mechanism.

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