Prototype of time digitizing system for BESIII endcap TOF upgrade*

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Abstract: The prototype of a time digitizing system for the BESIII endcap TOF (ETOF) upgrade is introduced in this paper. The ETOF readout electronics has a distributed architecture. Hit signals from the multi-gap resistive plate chamber (MRPC) are signaled as LVDS by front-end electronics (FEE) and are then sent to the back-end time digitizing system via long shield differential twisted pair cables. The ETOF digitizing system consists of two VME crates, each of which contains modules for time digitization, clock, trigger, fast control, etc. The time digitizing module (TDIG) of this prototype can support up to 72 electrical channels for hit information measurement. The fast control (FCTL) module can operate in barrel or endcap mode. The barrel FCTL fans out fast control signals from the trigger system to the endcap FCTLs, merges data from the endcaps and then transfers to the trigger system. Without modifying the barrel TOF (BTOF) structure, this time digitizing architecture benefits from improved ETOF performance without degrading the BTOF performance. Lab experiments show that the time resolution of this digitizing system can be lower than 20 ps, and the data throughput to the DAQ can be about 92 Mbps. Beam experiments show that the total time resolution can be lower than 45 ps.

Key words: BESIII, endcap upgrade, time-of-flight, high precision time measurement, readout electronics

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1 Introduction

BEPC II [1] has been running since the summer of 2008, and the luminosity has been continuously improving to about $6.5\times10^{32}\mathrm{cm}^{-2}\cdot\mathrm{s}^{-1}$, which makes it possible for the BESIII detector to operate correctly and efficiently [2]. The BESIII TOF (time-of-flight) system is based on plastic scintillator bars read out by fast fine mesh photomultiplier tubes (PMTs). It consists of a barrel and two endcaps [3]. The major physics goal of the TOF is particle identification (PID), which plays an essential role in the study of τ-charm physics. The PID capability is determined by the resolution of the time measurement. The current time resolution of the TOF system is about 92 ps in the barrel and 138 ps in the endcaps for π, corresponding to an average K/π separation (2σ) of around 1.1 GeV [4]. To further improve the BESIII PID capability, the resolution of the endcap TOF (ETOF) is planned to be upgraded to about 80 ps, corresponding to 1.4 GeV K/π separation (2σ), which will make BESIII a world-class detector, sufficient to identify charged particles over the entire momentum range of interest. The physics goals require each ETOF channel to have a total time resolution of better than 80 ps, of which only 25 ps should be contributed by the electronics.

To achieve this goal in the upgrade program, the newly developed and widely used gaseous detector technology, the multi-gap resistive plate chamber (MRPC) [5–7], was chosen for the ETOF detector, and an MRPC prototype with pad readout was developed. It is configured into a trapezium shape with 2·12 readout pads, each of which supports a signal readout from both sides [8]. There will be 36 MRPCs for each endcap, corresponding to 864 electrical channels, respectively. However, the original number of channels before the upgrade was only 48 for each endcap. The basic principle of the upgrade is to replace only the ETOF components with new ones while keeping other BESIII detector systems unchanged. Facing the restrictions of front-end circuit size, design cost and complexity caused by the greatly increased number of electrical channels, the lumped design methodology with long (∼18 m) analogue signal trans-

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mission used in the barrel TOF (BTOF) should [9] be replaced by a distributed system.

In the upgraded ETOF, the front-end electronics are separated from the time digitizing system and moved to the side of the detector. Special characteristics are needed to adapt the weak output charge signal from the MRPC (about tens of fC). An ultra-fast and low power front-end amplifier-discriminator ASIC with 8 channels per chip and a NINO [10] LVDS output driver is the best choice for the ETOF upgrade. It is designed for use with MRPC detectors. This distributed design methodology gives the maximum reduction in time resolution degradation from the electronics. Combined with the time over threshold (TOT) technique [11], time (T) and charge (Q) information of hit signals captured by the MRPC detector and digitized by HPTDC with 25 ps bins [12] can be achieved together during one measurement. The leading edge position of the input signal represents the hit time while the width between leading and trailing edges represents the charge for particle identifying. In the distributed scheme, the MRPC signal is amplified, shaped, discriminated, stretched and eventually converted into the LVDS signal. How to digitize signals from so many front-end electrical channels becomes a critical design challenge for the ETOF upgrade.

In this paper, a prototype of the time digitizing system was proposed and developed for the ETOF upgrade. To verify the performance of time measurement resolution and data transmission, some experiments were performed.

2 Architecture of time digitizing system

The original BESIII TOF readout system [9] consists of two VME crates, each of which contains 11 barrel and three endcap TOF-FEE modules. The barrel and endcap modules are designed with the same circuit board formation. The operating mode can be switched by writing different values into an on-board register. Besides FEEs, the readout system also contains FEE rear (FEE_Rear), fast control (FCTL) and clock modules. To ensure that the ETOF upgrade meets the requirement of signals read out from 1728 rather than 96 electrical channels, the ETOF readout modules are moved out of the original VME crates (now called BTOF crates) and rearranged into two new so-called ETOF crates, together with the corresponding clock and fast control modules. After this rearrangement, the BTOF crate-A, located on the 3rd floor of the BESIII electronics building, contains the original FEEs [9], FEE_Rears, TOF monitor [13], master clock [14] and PowerPC control modules. The BTOF crate-B, which is located on the ground floor, is unchanged except for the lack of three ETOF modules.

As mentioned above, the ETOF readout electronics have a distributed architecture. The FEEs are moved to the front-end detector side, leaving the time digitizing modules (called TDIG) residing in the ETOF crates. For the purpose of interacting with the trigger system, each ETOF crate contains an extra fast control module besides the TDIGs. For the purpose of system level clock synchronization, a slave clock module is also required in

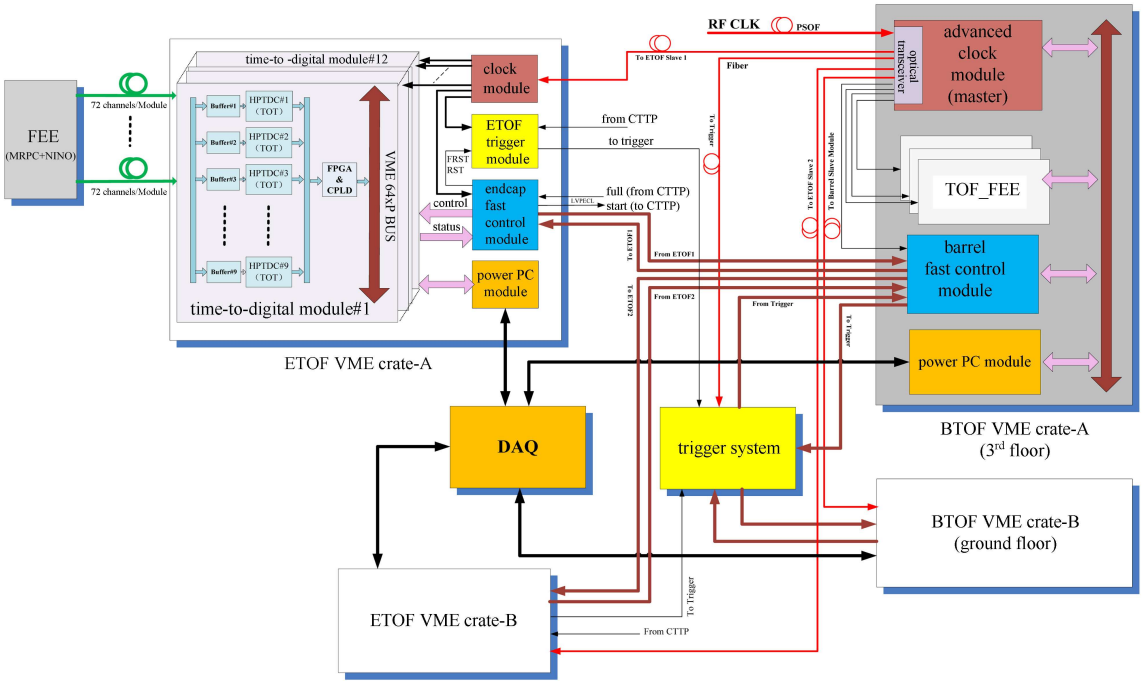

Fig. 1. The architecture of the time digitizing system for the ETOF upgrade.

each ETOF crate. It receives clock information from the master clock module located in BTOF crate-A. To minimize modification of the original BESIII structure and to guarantee system level reliability, the trigger system hardware and IO interfaces are unchanged except for minor logic and algorithm fixes. The BESIII trigger system can only interact with two FCTL modules, so the FCTL module in BTOF crate-A has to be redesigned. It is set up as a router to transfer signals from FCTLs in the ETOF crates to the trigger system. The FCTL in BTOF crate-B is unchanged.

Figure 1 schematically shows the structure and interfaces of the ETOF time digitizing system. In this upgrade scheme, the BTOF VME modules housed in crate-B, placed on the ground floor, including FEE (rear), monitor, clock and fast control modules, remain unchanged. The advanced clock module [14] plugged into BTOF crate-A, located on the 3rd floor, receives a 500 MHz RF clock from the BEPC II accelerator via a phase stabilized optical fiber (PSOF), and executes the tasks of TOF clock generating, synchronizing and distribution. It fans out 15 clock signals with LVPECL and five with optics. Slave clock modules plugged into the ETOF crates receive the synchronized and stable clock from the master through optical fiber channels. The BTOF crate-A clock module also fans out 18 LVPECL clocks to feed other modules inside the same ETOF crate and two optical clocks for backup or expansion.

During operation, the ETOF trigger module generates trigger conditions according to signals from CTTP (coincide, threshold, test and power) modules and sends them to the general trigger system for trigger selection. Due to the difference between MRPC and PMT installation, the trigger algorithms for the ETOF should be modified and implemented in the ETOF trigger modules [15].

For the purpose of calibrating the front-end electronics, the ETOF FCTL module sends a calibrating start signal to the front-end and then generates a pseudo L1 fast control signal to the TDIG modules to simulate the trigger arriving. Once the start signal is received, each FEE generates a step signal feeding to a discriminator to simulate a hit event. The delay between the start and L1 leading edge can be adjusted by the DAQ.

In this upgrade scheme, compared with the BESIII TOF readout electronics [9], the BTOF electronic modules are almost unchanged, which guarantees the original BTOF measurement performance. The design of the readout architecture and ETOF time digitizing system are also simplified. To avoid the risk of clock performance degradation, the original BESIII clock distribution scheme is reserved with some minor alterations.

In addition to the BTOF electronics, there are two extra VME crates for the ETOF upgrade. The front-end electronics and time digitizing system are separated but connected to each other via long cables. The large increase in the number of electrical channels, detached architecture and newly designed VME modules make it necessary to evaluate the resolution of time measurements and the performance of the DAQ in transmitting VME data.

3 Time digitizing module design

To evaluate the time digitizing resolution, a 9U VME prototype module called TDIG is developed [16]. Each TDIG module receives 72 channels of time signal from three MRPC detectors via three individual high speed and high density shield differential twisted pair cables [17], respectively. The cable length is about 10 m. Fig. 2 shows the TDIG module structure.

To support up to 72 electrical channels, each TDIG needs a total of nine HPTDCs. The TDCs are divided into three groups, each of which is formed into a daisy chain for the purpose of configuration or status checking through the JTAG interface. Configuration data sent from the DAQ is received via the VME bus and buffered into local memory in the Configure & Status Extract module. Once the configuration command arrives, JTAG Ctrl sub-modules in the FPGA read out these data and feed to HPTDC via the JTAG ports. These three JTAG Ctrl modules operate synchronously, which means that these three groups of HPTDCs are configured simultaneously. In addition to configuration, the JTAG Ctrl modules also collect TDC status information including error, token, FIFO, trigger or DLL etc, through the JTAG ports. According to the needs of the experiment, status information (such as FIFO status indicating whether there is TDC overflow or not) can be fed to the TDIG Status Monitor module to generate a fast control signal, which is then sent to the BESIII fast control system.

In the case of time measurement, to avoid degradation of LVDS signal quality caused by the long transmission cables, and to improve the ability to drive the TDCs, LVDS buffers (for simplicity, not shown in Fig. 2) are adopted before the signal enters the TDC. After being configured correctly, HPTDC enters into the very high resolution mode for time measuring, with 25 ps bin size. Once a hit signal occurs on any HPTDC channel, it will be latched with coarse counter and fine calibration values and stored in the L1 buffer together with its channel identifier, waiting for L1 trigger selection. The L1 buffer, with a depth of 256 words, is shared with eight channels. The total time measurement is encoded into a binary format. FCTL modules in the BTOF or ETOF crates fanout the L1 trigger signal generated from the BESIII trigger system to each TDIG module. The TDIG

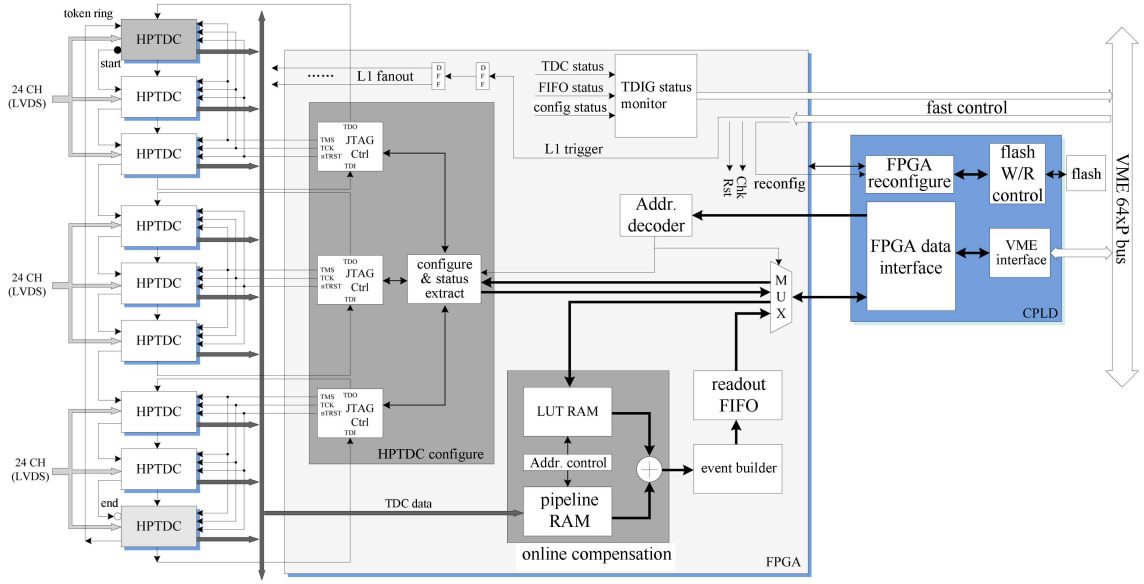

Fig. 2. Structure of TDIG module.

receives the L1 trigger signal from the fast control system and then fans out further to feed to the trigger input port of each HPTDC, respectively. The mismatch between a real physical event occurring (T0) and the trigger input time, caused by trigger latency, can be eliminated by a trigger matching mechanism, where the HPTDC searches hit information in the L1 buffer and commits as valid only if this hit information is within a pre-set time range called the match window [12].

In the case of data readout, all HPTDCs are configured into a daisy-chain formation on which a token is transferred. For the purpose of fixing the token starting location, the HPTDC on the topside is appointed as the master TDC and designated No. 1. The downside TDC, where the token ends, is designated No. 9. All TDCs are configured into parallel readout mode so that they share a common 32-bit bus for data readout.

Benefitting from the R-C delay line and data interpolation, the HPTDCs can achieve an excellent measurement resolution of 25ps. However, due to variations in processing, the R-C delay line has large dependencies on processing parameters and each TDC chip needs to be calibrated. The purpose of calibration is to eliminate the integral non-linearity (INL) in the raw data if the INL can be obtained prior and the value is fixed [16]. Actually, the R-C delay line in the HPTDCs has very small dependencies on temperature and supply voltage, which gives a fixed INL for each channel. With software algorithms, we can easily compute and obtain the INL values corresponding to the raw measurements. In Fig. 2, we store the INL values obtained before calibration into the FPGA LUT-RAMs through the DAQ. During calibration, the TDIG will compensate the raw data of each online channel by combining the INL value corresponding to this channel.

The calibrated hit measurements are fed to the event builder module for event building before being stored in the event FIFO to wait for readout to the DAQ via the VME bus. To improve the reliability and portability, all operations corresponding to the VME are implemented in a CPLD chip. Besides, for the purpose of flexibility, CPLD also has the ability to reconfigure the FPGA logic. The new logic data transmitted from the DAQ is stored in flash storage that is controlled by the CPLD.

4 Fast control module design

The fast control (FCTL) system in the TOF electronics fans out fast control signals, such as L1 triggers and system reset signals sent from the trigger system, to each VME TOF module including the BTOF FEE and ETOF TDIG. Meanwhile, the FCTL collects the status of the TOF readout modules and sends the information back to the trigger system. Fast control signals can be classified into 3 groups: trigger, control and status signals. The new TOF FCTL system consists of 4 VME modules plugged into 4 BTOF and ETOF crates respectively. As well asthe unchanged BTOF FCTL module on the ground floor of the BESIII building, there are 3 newly developed FCTL modules, 1 of which is set up as master or router in BTOF crate-A (3rd floor), and 2 of which are set up as slaves in 2 ETOF crates respectively. To simplify the design and use of the FCTL, the master FCTL module has the same hardware structure as that of the slaves. Fig. 1 shows the connection between FCTL

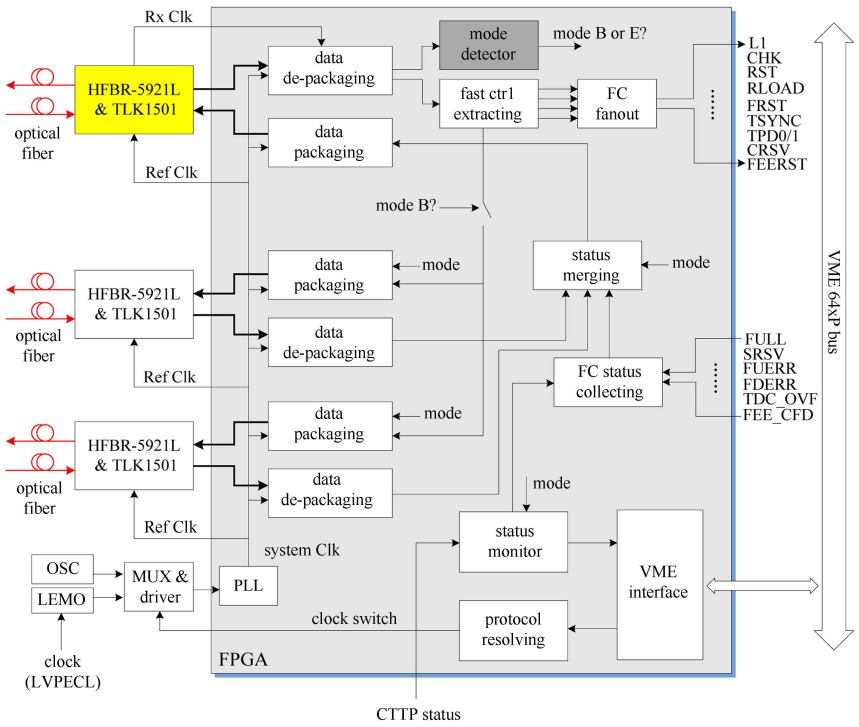

Fig. 3. Structure of fast control module.

modules and their locations. Fig. 3, below, shows the structure of the FCTL module.

There are a total of four optical fiber pairs per FCTL module, with full duplex Rx and Tx channels. There are two different FCTL operating modes, which are the BTOF mode and the ETOF mode. In the case of the BTOF mode, three pairs are used and one pair is reserved for backup. In the case of the ETOF mode, one pair is used and three pairs are for backup. The topside optical pair is appointed as a master pair, whichever mode is being used. During operation, the BTOF FCTL communicates with the trigger system through the master pair, and the ETOFs communicate through the two slave pairs. Unlike the original BTOF FCTL [9], the new FCTL module can switch to BTOF or ETOF mode automatically. Before operation, the FCTL module detects the mode, BTOF or ETOF, according to the mode information embedded in the data stream it receives. If it detects that the received data is sent from the trigger system, then the FCTL switches to BTOF mode. If the signal is from the BTOF FCTL, then it switches to ETOF mode. In BTOF mode, the FCTL extracts fast control information from the trigger system and then fans out to the BTOF FEE modules via the VME bus, and to the ETOF FCTL modules via the two slave optical fiber pairs embedded with BTOF mode information. In ETOF mode, the FCTL extracts and fans out fast control to the TDIG modules without fanning out via slave fiber pairs, which are disabled in this mode. On whichever BTOF or ETOF FCTL FPGA, there is a logic module collecting fast control status sent from TOF readout modules. The fast control status from the BTOF is sent back to the trigger system merged with that of the ETOFs. For the purpose of diagnostics or monitoring, FCTL or CTTP status monitoring data can be embedded into the fast control status stream.

5 Experiments and verification

The time measuring resolution plays an essential role in BESIII PID and is naturally designated as a key TOF electronic specification for continuous improvement. Differing from the BTOF, the ETOF upgradescheme adopts a distributed design methodology, which simplifies the FEE design, but this means that the new timing resolution is unknown. The design value for electronic resolution is an RMS value of about 25 ps. On the other hand, the sharp increase in the number of electrical channels gives a higher requirement for data transmission to DAQ than was previously the case for the BTOF. To evaluate the time digitizing resolution and data transmission performance, some experiments and verifications were carried out.

5.1 Data transmission evaluation

To search the hit position precisely and efficiently,

the match window of the HPTDC is set to be 3 μs, which is nearly half the BESIII 6.4 μs trigger latency. Due to the rarity of multi-hitting in this time slot, the default hit number for each electrical channel is assigned to be 1 while evaluating the output data amount. So we can obtain the following total output words (32bit) for each TDIG module:

$$72\text{ch}\times\text{hit occupancy}\times 2\times\text{hit num}+4,$$

where 2 is for the leading and trailing edges for TOT application, and 4 is for redundant data packaging information. Table 1 shows the relationship between detector hit occupancy and ETOF electronic module data output.

Table 1. Relationship between occupancy and ETOF data.

hit occupancy (%)	hit ch nb per TDIG	max event size per TDIG (byte)	max event size per crate (byte)	output data rate/crate (Mbytes/s)
100	72	592	7104	28.416
50	36	304	3648	14.592
25	18	160	1920	7.68
11.1	8	80	960	3.84
5.6	4	48	576	2.304

In the case of 25% occupancy for ETOF, which is greater than the average level for BESIII experiment, the hit channel number of each TDIG module is 18, corresponding to an event size of 160 bytes for each TDIG and 1920 bytes for each ETOF crate. Due to the 4000 Hz average trigger rate, the data throughput for each crate should then be greater than 7.68 Mbyte/s. So a VME processor module with a 100 Mbps Ethernet port (e.g. MVME5100) is enough for the ETOF VME to create a data readout. To read digitized hit information out as soon as possible, the ETOF crate adopts a chained block transfer (CBLT) DMA technique to transmit data from the 12 TDIG modules.

To evaluate the performance of VME data transmission, we designed the following test bench software, shown in Fig. 4. There are two major modules, which are the command & network (Cmd & Net) module and the hardware interaction module. This runs on MVME5100 under VxWorks, a real-time embedded operating system. The Cmd & Net module performs the tasks of network communication and command execution. The hardware interaction module, which is device driver related, executes the tasks of hardware configuration and control (using a VME bridge chip called universe2 that executes all VME bus operations), and CBLT DMA handling.

The experiment showed that the data throughput of the VME bus can reach up to about 30 Mbyte/s and that of 100 M Ethernet interface on MVME5100 up to about 92 Mbps. This result can meet the requirement of the ETOF upgrade data transmission.

5.2 Time digitizing INL evaluation

To evaluate the time digitizing INL, we used a statistical code density test based on a source of random hits [18] and achieved the INL curve shown in Fig. 5. The INL is in the range of −2–9 LSB.

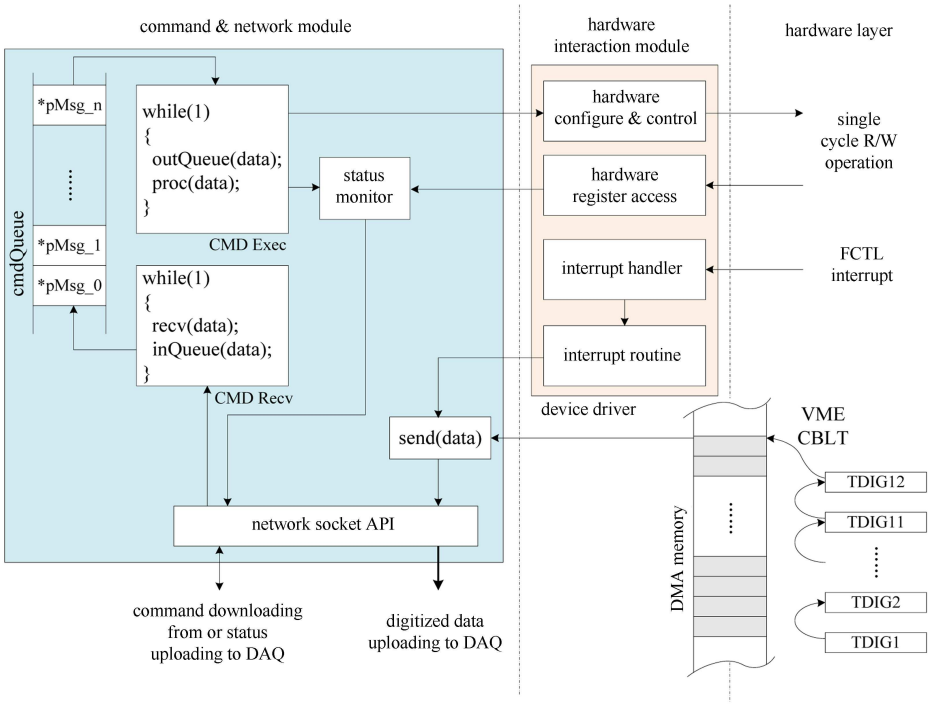

Fig. 4. Structure of VxWorks real-time software on VME single computer MVME5100.

5.3 Time digitizing resolution evaluation

To evaluate the time measurement resolution, we used the conventional cable delay method [16], both with and without FEEs. Fig. 6 shows the time measurement resolution without FEEs while varying the cable delay value for different HPTDCs. The test signal was generated by a TEK AFG3252 and passed to the LVDS by a converter board. The resolution is achieved by measuring the time interval for two different channels. According to Fig. 6, the resolution is better than 20 ps, which can meet the required 25 ps for the ETOF upgrade.

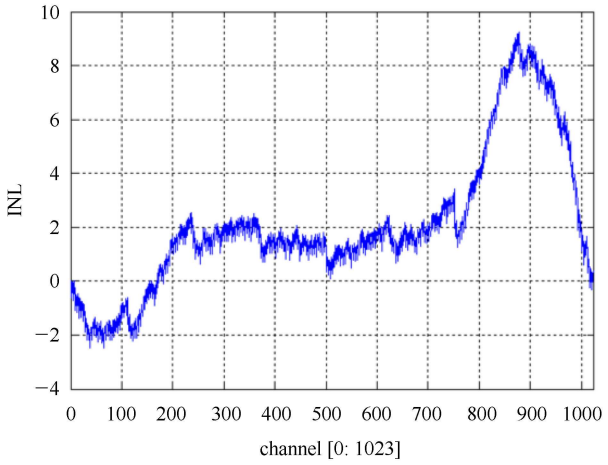

Fig. 5. INL curve of time digitizer.

To evaluate the measurement resolution with FEEs, we fed the test signal to FEEs for discriminating and LVDS signaling, and measured the delay time of two randomly selected channels of one HPTDC. We then obtained the statistical histograms shown in Fig. 7. Fig. 8 shows the obtained resolution of all HPTDC digitizing channels on one TDIG module.

According to Figs. 7 and 8, we can conclude that this time digitizing prototype can achieve good measuring resolution, better than 25 ps, with FEEs connected.

5.4 Beam test

Besides the experiments above, we have also performed a beam test in IHEP, June 2011, to evaluate the total time measurement resolution. Fig. 9 shows the test configuration schematic. To reduce the cosmic background, two scintillators were located along the beam direction. The coincidence unit will generate a signal used as the trigger for the beam test if there is a valid beam signal passing through these two scintillators.

Figure 10 shows the total measuring resolution [16], from which we can conclude that the time digitizing electronics can achieve a good timing resolution of 45 ps, which is better than the ETOF upgrade design value of 60 ps. Furthermore, we can also conclude that the total timing resolution is insensitive to the hit position.

To evaluate the total time measuring resolution contributed by electronics with or without beam, another

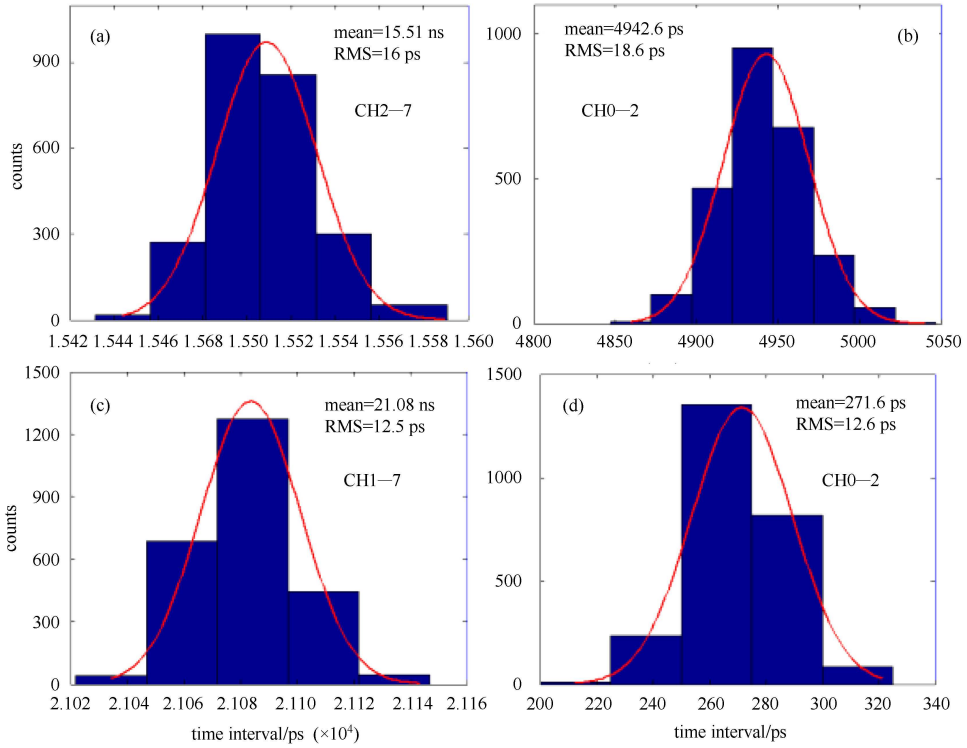

Fig. 6. Time measuring resolution for different HPTDCs (without FEE). (a) HPTDC0; (b) HPTDC1; (c) HPTDC5; (d) HPTDC8.

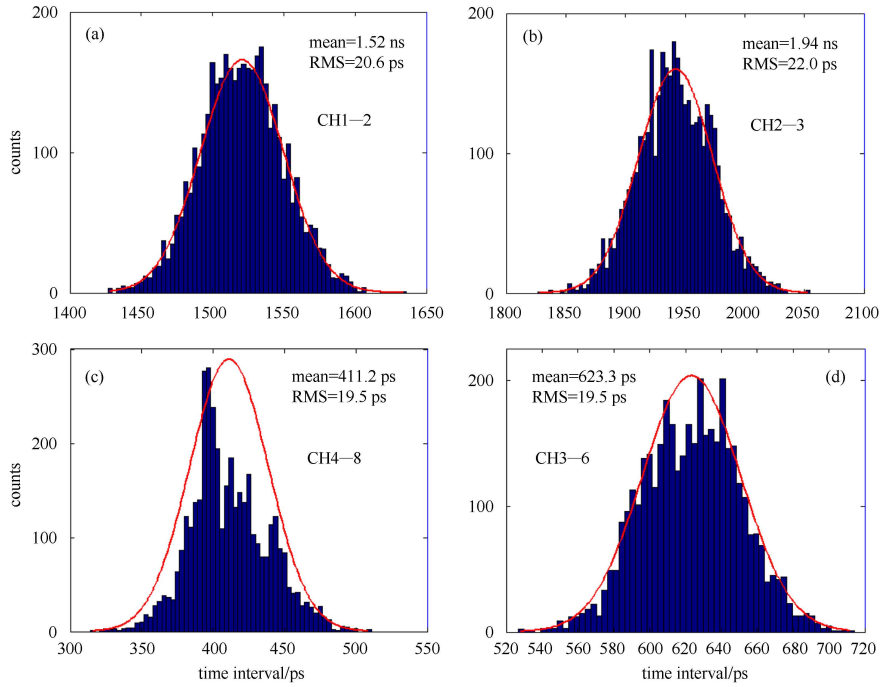

Fig. 7. Time measuring resolution for different HPTDCs (with FEEs). (a) HPTDC2; (b) HPTDC3; (c) HPTDC4; (d) HPTDC8.

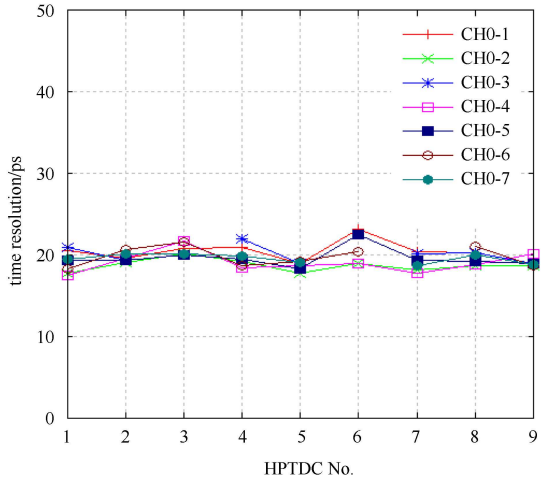

Fig. 8. Time measuring resolution (with FEEs) for all channels of a TDIG module.

beam test was performed in June 2012. The results are shown in Fig. 11, where the marker (0) represents the test without beam and (1) with beam. According to Fig. 11, we can conclude that the total timing resolution contributed by the electronics is better than 25 ps, except for that of HPTDC1. The measured resolution of even-to-even channels is obviously worse than that of even-to-odd ones. Because the previous tests show no signs of problems with this HPTDC, this is probably caused by an improper electrical connections somewhere. Further beam tests will be performed to verify this.

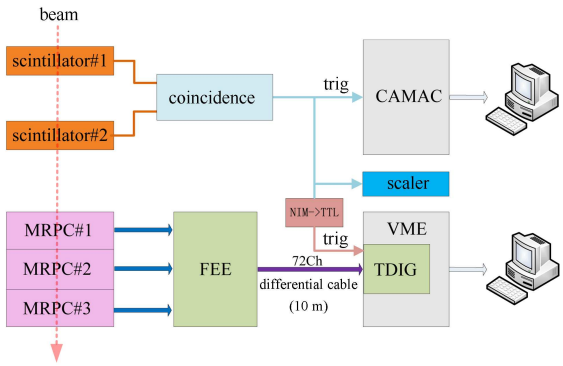

Fig. 9. Beam test configuration.

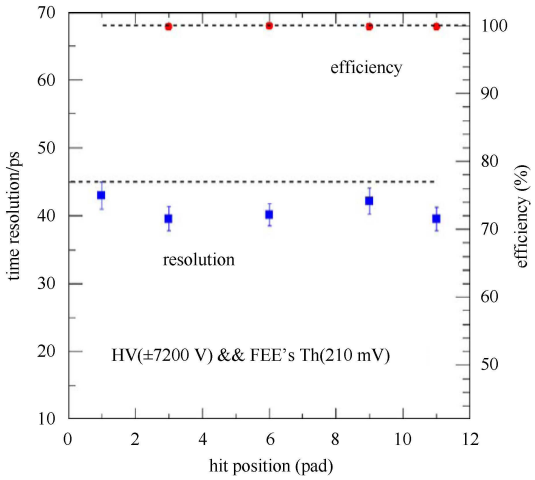

Fig. 10. Beam test result in June 2011.

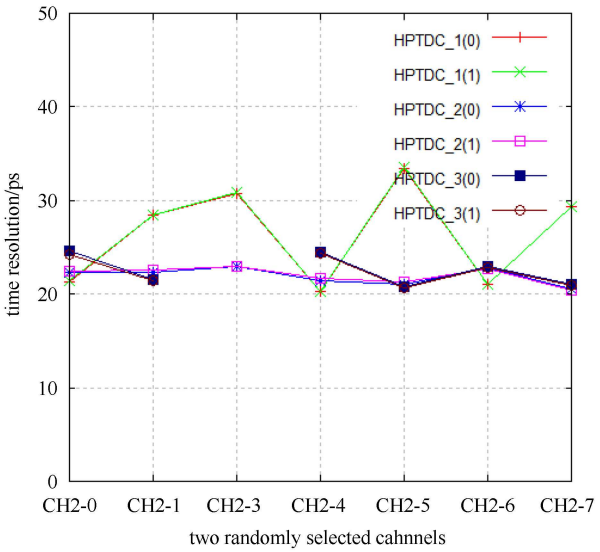

Fig. 11. Time measuring resolution contributed by electronics, with or without beam.

6 Conclusions

A prototype time digitizing system for the BESIII ETOF upgrade has been designed and introduced in this paper. The prototype has a distributed structure that makes it possible and reliable to read the signal from a greatly increased number of electrical channels from the ETOF MRPC detectors via long differential twisted pair cables.

There exist two VME crates for the ETOF upgrade, each of which contains 12 time digitizing modules (TDIG), 1 slave clock module, 1 fast control module (FCTL), 1 ETOF related trigger module and 1 bus controller module (MVME5100). All TDIG modules transfer digitized time information to the controller through CBLT DMA transactions initiated by the FCTL. The meticulously designed embedded real-time VxWorks software on the VME controller receives the digitized data from the VME bus and transfers them to the DAQ through 100 M Ethernet.

To evaluate the performance of this prototype, experiments were performed with and without FEE, and with and without beam. The experimental results show that the total data readout throughput of one VME crate can reach up to about 92 Mbps, which is similar to that of the Daya Bay experiment DAQ [19, 20]. The time measuring resolution can be better than 20 ps without FEEs, 25 ps with FEEs and 60 ps with beam test. According to the experiments, we conclude that this time digitizing prototype system can meet the requirements for the ETOF upgrade physics goals for particle identification.

We will now focus on integrating the system with the BTOF, trigger system and DAQ of BESIII, as well as optimizing the design of the VME readout module, including its mechanical structure, reliability and consistency. We also need to manufacture modules and carry out short and long-term experiments and tests before installing them into BESIII.

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