

Proposal of the readout electronics for the WCDA in the LHAASO experiment^{*}

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Abstract: The LHAASO (Large High Altitude Air Shower Observatory) experiment is proposed for a very high energy gamma ray source survey, in which the WCDA (Water Cherenkov Detector Array) is one of the major components. In the WCDA, a total of 3600 PMTs are placed under water in four ponds, each with a size of 150 m×150 m. Precise time and charge measurement is required for the PMT signals, over a large signal amplitude range from a single P.E. (photo electron) to 4000 P.E. To fulfill the high requirement of a signal measurement in so many front end nodes scattered in a large area, special techniques are developed, such as multiple gain readout, hybrid transmission of clocks, commands and data, precise clock phase alignment and new trigger electronics. We present the readout electronics architecture for the WCDA and several prototype modules, which are now being tested in the laboratory.

Key words: WCDA, LHAASO, readout electronics, PMT

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1 Introduction

Gamma ray source detection above 30 TeV is an encouraging approach for finding galactic cosmic ray sources. An all sky survey for gamma ray sources is essential for population accumulation for various types of sources above 100 GeV [1]. To target these goals, the Large High Altitude Air Shower Observatory (LHAASO) [1, 2] is proposed, with multiple air shower detection techniques combined together. As shown in Fig. 1, the LHAASO mainly consists of a KM2A (1 km² complex array), a WCDA (Water Cherenkov Detector Array) [3, 4], a WFCTA (wide FOV Cherenkov telescope array) and a SCDA (high threshold core-detector array).

As one of the major components in LHAASO, the WCDA consists of four 150 m×150 m ponds, as marked by the four octagons in Fig. 1, thus a total area of 90000 m² is covered. Every pond incorporates 900 detector cells (5 m×5 m), each with one photomultiplier tube(PMT) looking up at the bottom center to collect the Cherenkov light produced by the shower particles in water. This detector array of 900 cells is partitioned into 10 × 10 detector units, as shown in Fig. 2. Each unit contains 3×3 PMTs and their outputs are fed to one front end electronics module (FEE) for charge and time information measurement.

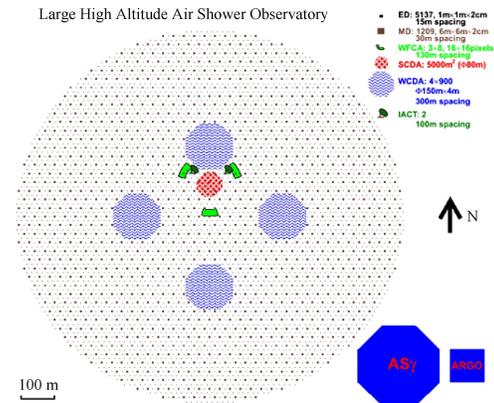


Fig. 1. Layout of the LHAASO array.

Both precise time and charge measurement is required in the WCDA readout electronics. We need to read out a total of 3600 PMT channels scattered within a large area and the RMS of time measurement is required to be better than 0.5 ns, which means precise clock distribution and phase alignment on a large scale is paramount. Besides, data, commands and clocks need to be transferred over a long distance (hundreds of meters), so the transmission quality and the system complexity are great concerns. To reduce the number of signal cables, we decided to propose a new architecture instead

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of employing the traditional trigger structure that requires receiving hit information from front ends and feeding trigger signals back. Furthermore, the large input dynamic range (1–4000 P.E.) is also a great challenge, compared with the readout electronics for the WCDA in other experiments [5, 6].

The measurement requirement of the readout electronics is listed in Table 1.

Table 1. Measurement requirement of the WCDA readout electronics.

item	requirement
bin size of time measurement	<1 ns
RMS of time measurement	<0.5 ns
dynamic range of time measurement	2 us
minimum interval of two hit signals	100 ns
dynamic range of charge measurement	S.P.E. ~4000 P.E.
resolution of charge measurement	30%@S.P.E.; 3%@4000P.E.
channel number	3600

Considering the situation in the read out of the WCDA in LHAASO, the following difficulties needs to be overcome with novel methods and techniques:

- 1) precise time and charge measurement over an ultra large dynamic range;
- 2) high-quality clock distribution and phase alignment;
- 3) long distance transmission of clocks, commands and a huge amount of data;
- 4) new trigger electronics design.

2 Architecture of the WCDA readout electronics

The architecture of the WCDA readout electronics is shown in Fig. 3. For each WCDA pond, 100 front end electronics modules are located above water, very

close to the PMTs. Each FEE is responsible for the signal readout for nine PMTs within one detector unit in Fig. 2. The signal from the PMT is directly digitized by the FEE and then transmitted to the clock and data transferring module (CDTM) in the control room. Signal transmission is based on fibers (hundreds of meters long) to guarantee a good transmission quality. Special methods are applied to address the issue of a large dynamic range in FEEs, which will be presented in posterior sections.

Each CDTM collects data from ten FEEs and then transfers the data to the trigger module; it also functions as the bridge for communication between the FEEs and the control system for transferring commands as well as system monitoring. Due to the complicated phenomena of cosmic ray showers, a high flexibility of trigger electronics is required to accommodate different potential trigger patterns. Invoked by the “triggerless” idea, we propose a new trigger electronics structure to achieve a good flexibility.

As mentioned above, a high time measurement resolution better than 1 ns is required over all the 3600 FEE channels. Therefore, we need to achieve a high quality clock distribution. Based on a simplified White Rabbit

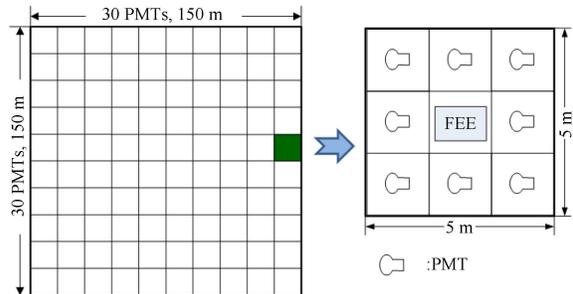


Fig. 2. Structure of one WCDA pond in LHAASO.

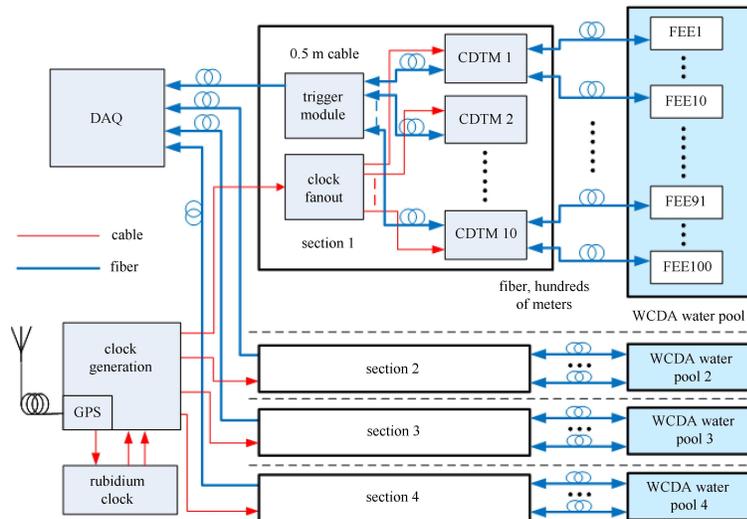


Fig. 3. Architecture of the WCDA readout electronics.

(WR) protocol [7–9], we employed an adaptive phase adjustment method to precisely align the clock phases. Besides, absolute time information needs to be included in the measurement results to identify an air shower event. We receive the signal from the global positioning system (GPS) and use it to discipline a rubidium clock source to generate the system clock reference, as shown in Fig. 3. Detailed information is included in the following sections.

2.1 Measurement method of the PMT signal with an ultra large dynamic range

The PMT signal amplitude would vary from 1 P.E. to 4000 P.E. while the discrimination threshold is as low as 0.25 P.E. It means that a resolution of 16 bits is required on the overall system performance, which is very difficult to achieve. To guarantee a good measurement resolution, especially for small signals (~ 1 P.E.), we employ two readout channels for each PMT: one is for the anode and the other is for a dynode (e.g. Dynode 10), as shown in Fig. 4.

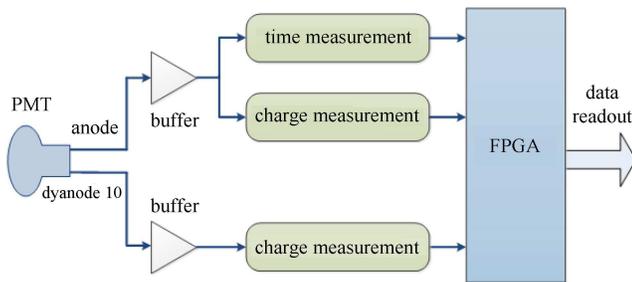


Fig. 4. Readout of the PMT signal.

By adjusting the gains of the buffers in the two readout channels, the anode channel can effectively cover a range of 1–133 P.E. while the Dynode 10 channel covers a range of 30–4000 P.E. A total dynamic range of 4000 is achieved and there exists enough overlap between the two channels. Since the dynamic range has been reassigned to two smaller scales, the requirement on the electronics

is greatly reduced. The PMT signal from the anode is also used for time measurement. After passing through the discrimination circuits, the hit signal is digitized by a Time to Digital Converter (TDC) integrated in the FPGA.

As for precise charge measurement, we can employ the digital peaking method, in which the PMT is digitized by an ADC after amplification and shaping, then the peak value of the amplitude can be sought based on the digital signal processing. We have worked on the measurement scheme [10–13] and finished the design of an FEE prototype based on this method, as shown in Fig. 5. The performance tests in the laboratory are underway.

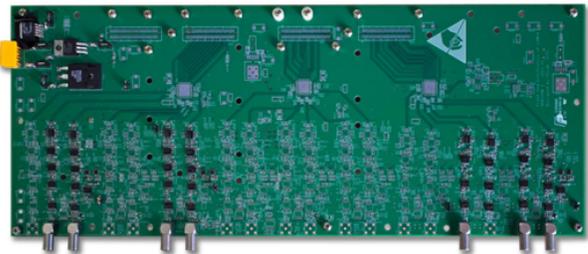


Fig. 5. Photograph of the FEE prototype.

Besides, we are also considering applying the Time-Over-Threshold (TOT) method in the signal measurement and integrating the circuits within an ASIC (application specific integrated circuit) chip. The ASIC design is also in process.

2.2 High quality clock distribution over a large area

Since the FEEs are distributed over a large area, the delay difference among the long signal transmission paths would cause non-aligned phases between the clock signals of different FEEs, which cannot be tolerated in high resolution time measurement. Besides, aging of the electronics and temperature variation would lead to fluctuation of the time delay. Thus, a precise real-time delay calibration and adjustment is needed.

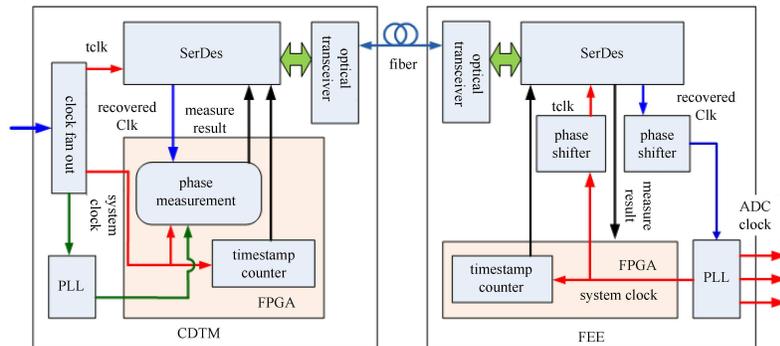


Fig. 6. Block diagram of the clock distribution and delay compensation method.

A novel technology named White Rabbit [7–9] (WR) has recently been developed in the frame of CERN’s (and GSI’s) renovation projects. It is capable of controlling thousands of nodes over a few kilometers with a good timing accuracy. As for the timing, its kernel technique is based on the Precision Time Protocol (PTP, IEEE1588) and the Synchronous Ethernet technology. Invoked by the WR technique, we employ an adaptive delay measurement and compensation structure, as shown in Fig. 6.

As aforementioned, each CDTM communicates with ten FEEs over a distance of hundreds of meters. The CDTM (as the master) distributes the clock signals to the FEEs (as the slaves). Real-time phase measurement is implemented in an FPGA based on the digital dual mixer time difference [14] (DMTD) measuring method. To further enhance the measurement resolution, an FPGA based TDC (resolution ~ 1 ns) is used. The phase measurement results are sent to the FEEs, in which the clock signal is adjusted for phase alignment. A digitally controlled phase locked loop (PLL) and precise delay line ASICs are used to achieve a tuning step of around 10 ps.

As a high-quality timing system, all the FEEs are required to be initiated and started at a precisely matched time point, which means a global reset must arrive at all the FEEs simultaneously. This is done in two steps. First, the clock signals are well aligned using the method just mentioned above. Second, a special timing sequence is designed, as shown in Fig. 7. The master (CDTM) sends a ‘Reset’ pulse just after the PPS (pulse per second) signal. When this reset signal is detected by the slave (FEE), a flag named ‘Reset ready’ is asserted, with which the local reset signal in the slave can be generated after the next PPS signal is detected. To guarantee a synchronous reset of all the slaves, it is required that the uncertainty of the PPS signal is within one system clock cycle, while the uncertainty of the reset signal from the master can be as large as 1 s, which can be easily achieved.

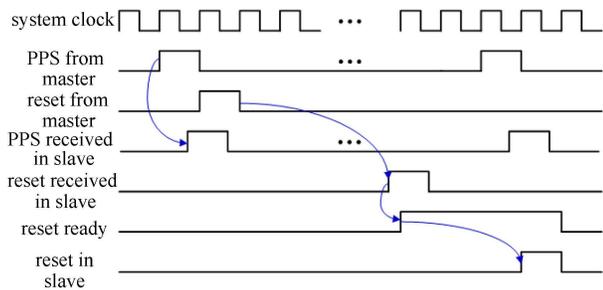


Fig. 7. Timing sequence for a global reset.

Besides, the CDTM is also responsible for collecting data from the FEEs and transferring them to the trigger processing electronics. Considering an average raw event

rate of 50 kHz, the total data rate for each CDTM would be as high as $50 \text{ kHz} \times 96 \text{ bit (packet size)} \times 9 \text{ (FEE channel number)} \times 10 = 432 \text{ Mbps}$. Considering the cost of 8 b/10 b encoding [15], the data rate is around 540 Mbps. Fibers are employed to achieve such a high transmission speed. Meanwhile, data, commands and clocks are mixed together in the fiber based transmission line, so a good system simplicity is guaranteed.

2.3 New trigger electronics design

In traditional trigger electronics, such as in AMANDA [16] and in BESIII [17], hit signals are collected from FEEs for trigger processing and global triggers need to be sent back to front ends for data readout. The complex phenomena of cosmic ray showers require highly flexible trigger electronics, which can be modified online to accommodate different potential trigger patterns.

Invoked by the ‘triggerless’ idea [18, 19], we employ a new structure of trigger electronics. Complete data packets are collected from all the FEEs for trigger processing, so much more detailed information can be utilized to achieve a better trigger flexibility. Meanwhile, it also eliminates the need of feeding trigger signals back to front ends; thus a better system simplicity can be achieved. We plan to implement the triggerless idea with two potential methods. The first one is a completely triggerless design. All the data from the FEEs are processed by the software in the DAQ. A best flexibility can be guaranteed by this method, of course accompanied by the requirement of more resource cost on data storage and processing. In the second method, we consider designing a trigger module to collect all the data from FEEs and conducting real-time trigger processing within an FPGA device. The recent development of data transmission and FPGA techniques makes this feasible. The abundant programmable logic resources in the FPGA lead to a reconfigurable trigger electronics. Besides, since a large partition of fake events are rejected by the trigger electronics, the requirement on the DAQ is also reduced.

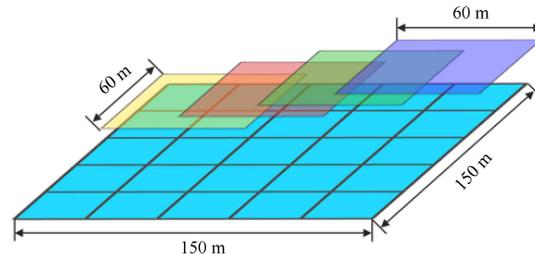


Fig. 8. Cluster arrangement for a basic trigger pattern.

We have finished the design of a trigger electronics prototype based on the second idea [20] and evaluate this design with a basic trigger pattern. As shown in Fig. 8, the PMTs within one pond are divided into 16

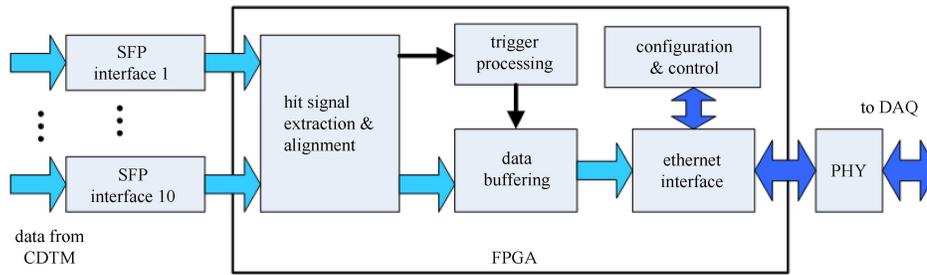


Fig. 9. Block diagram of the LHAASO trigger module.

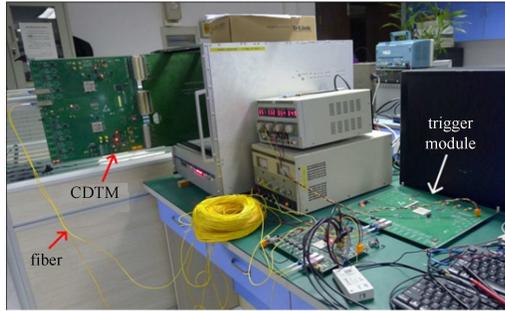


Fig. 10. System under test.

overlapped trigger clusters (each cluster is a 12×12 PMT array). When more than 12 PMTs in any cluster are fired within any 250 ns duration, it will be recognized as a valid event and a global trigger signal will be generated.

We implement the above trigger pattern with the logic design in one FPGA (Xilinx Virtex-6 xc6vlx240t), as shown in Fig. 9. Trigger processing and valid data selection are both integrated in the FPGA. One trigger module is required for each pond, which means the data from 100 FEEs are accumulated through ten CDTMs to this module, rendering a raw data rate up to 5.4 Gbps. Fibers are also used here to guarantee a high data trans-

fer rate.

Tests have been conducted on the data transmission performance and the validity of the trigger processing. Fig. 10 shows the system under test.

The aforementioned complete triggerless architecture is also under consideration.

3 Summary

The requirement and challenge of the WCDA readout electronics in LHAASO are introduced. To overcome the difficulties, we propose special techniques, such as multiple gain readout, hybrid transmission of clocks and commands & data, precise clock phase alignment and new trigger electronics. The architecture design of the electronics is presented in this paper. The technical design is in process and we have finished the design of several electronics prototypes, which are now being tested in the laboratory.

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