Design of a 1.2 GSPS single-channel real-time long-distance transmission sampling system for fast-transient signal

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Abstract This article has introduced the origin and speciality of fast-transient signal, and told the meaning of researching on fast-transient signal. The main troubles of sampling on fast-transient signal is its 'fast' and 'transient', and the experiment's bad condition also troubles the transmission of information. To solve those troubles we put forward a technology called 'digital Forward-sampling', and designs a sampling system for the fast-transient signal with this technology. The sampling rate of this system is 1.2 GSPS; it could get the whole pulse of fast-transient signal through the digital Forward-sampling technology; this system also could transmit the result to the analyzing equipment kilometers away immediately, before the data was destroyed by the electromagnetic and mechanical wave. In the end, this article tells the result of testing on this system, and gives the improved project.

Key words fast-transient signal, nanosecond, digital forward-sampling, real-time long-distance transmission

PACS 07.50.Qx, 29.85.Ca, 84.30.Sk

1 Introduction

Fast-transient pulse specifically refers to the transient electromagnetic pulse with rising time at nanosecond or sub- nanosecond order. This pulse signal is generated in technologies such as radioactive physical measurement, cosmic ray detection, etc. As the single fast pulse signal contains a plenty of physical contents related to ray particle beam. Recording the pulse waveform perfectly is of great significance for scientific research in such fields as Nuclear Power Industry, protection against radiation, high energy physics, etc.

Due to the non-repeatable time domain and fast pulse edge of single fast pulse, certain difficult has been brought for the record of pulse waveform. In addition, conditions on test site for generating single fast pulse are always very poor with great destructive electromagnetic and mechanical effects, which makes it necessary to timely transfer the results of pulse waveform record to the analysis device several miles away, so as to guarantee the security of test instrument and the personnel, and reduce the adverse impact of various effects on the information carried by the pulse waveform[1].

However, in our practices, it is found that the pulse waveform may generate aberrances due to the limitations of the transmission system in terms of pass band when single fast pulse obtained directly is transferred from test site to analysis device in the form of analog signal, thus damaging the information carried along with the pulse waveform[2].

The main reason why the information transferred in the form of analog signal is easy to be damaged is that the analog signal stores all information on the "form" of signal pulse. As the most important information is carried by each frequency component in the signal, the relative ratio of attenuation of different frequency components shall be different if the transport speciality changing with the input frequency. Thus,

Received 8 July 2008

aberrances shall be caused to the pulse "form" and the information carried by the pulse shall be damaged accordingly.

As per the theory of "analog-to-digital transformation", we have designed a set of collection system specific to the single fast pulse signal, so as to solve the problem of information acquisition ,which is mentioned above[3].

2 Principle of system design

2.1 Requirements on perfect system

To ensure all useful information before and after signal generation is acquired when conducting data collection towards single fast pulse signal, the common solution is to predict the fuzzy time range of signal generation first of all, and then start up the collection system in advance with abundant time margin left as per the predicted time range. Although intact pulse signal can be collected with this method, for fast signal with bandwidth at 100 trillion level, serious waste of system resources shall be caused by excessive margin time left for advance sampling if the predicted time range for signal generation is too fuzzy.

What's worse, the determination of margin time for advance sampling is almost impossible for some tests, e.g. cosmic ray detection, since the generation time of pulse signal is completely random. Besides, this method of single pulse collection cannot work independently but requires artificial control. Therefore, its applications in engineering are greatly restricted.

In engineering application, a perfect data collection system is the one that has been in the wait state from start-up and can automatically perform the sampling, storage, transmission and other procedures immediately upon the arrival of the signal to be measured, with the whole process independently conducted without artificial monitoring. The trigger mode of the collection system is named self-trigger. Self-trigger is the process in which the system starts up the sampling process when the voltage range exceeds the trigger threshold by comparing the voltage range of the measured signal itself and the trigger threshold of system trigger circuit. The major problem of the self-trigger mode lies in that the leading edge of the input signal before its voltage range reaches trigger threshold is missed when starting up the system, which shall lead to loss of key data.

As for this problem, lowering the trigger threshold of the system shall make no significance, and furthermore shall be restraint by the range of ground noise. The solution usually adopted is to divide the input signal into two roads: one touches off the system to start sampling and the other is input into the input end of A/D conversion chip as the measured signal。By delaying the measured signal to make it reach the A/D conversion chip a certain period of time later than the trigger signal, the leading edge of the measured signal can be colleted in an intact state.

However, additional trouble shall be added to the design process due to the problem of intact signal when collecting the single fast pulse. In addition, the delay process to high-frequency analog signal, either to add delay element or use sinuous delay line, may usually cause crosstalk or various kinds of additional noises, leading to unexpected aberrances of signal and sometimes even great bad results.

2.2 Actual system design

To meet the above-mentioned requirements, elaborate design should be pay more attention on two points for the collection system.

The first one is the advance sampling conducted to ensure all useful information is collected. Some commonly used schemes of advance sampling have been demonstrated in the text above but all of them fail to meet the three requirements mentioned above. Therefore, a more recent sampling scheme—digital advance sampling—is adopted by us. The working principle of the scheme is shown in Fig. 1.

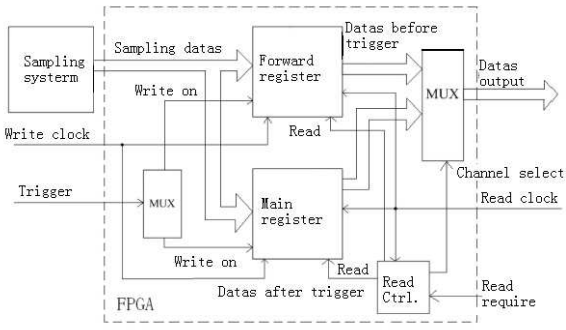

Fig. 1. Principle diagram of digital realization of advance sampling.

When the system is powered on, it shall start up sampling via external control signal and store all data collected in the prefix register first of all; cyclic storage of data shall be realized via control of the counter,

so that the data stored in the previous round is continuously covered by the digital signal input into the prefix register before the trigger signal (i.e. the measured signal) arrives. After the trigger signal arrives, the trigger module controls chip select signal and the prefix register stops writing, and hereafter all data shall be stored into the main register. When "read" signal arrives, data in the prefix register is taken out in sequence by determining the last write address of the prefix register; when all data in the prefix register are taken out, data shall be continuously withdrawn from the main register via chip select. Thus, waveform of the signal pulse before its voltage range arrives trigger threshold can be acquired completely, as long as the storage capacity of the prefix register is designed to be large enough. Through this, no additional noise or interference shall be added to the measured signal while advance sampling is fulfilled. To sum up, the three requirements for a perfect collection system of single fast pulse mentioned above are all complied with.

The second point is the real-time long-distance transmission design. For this, saving cost to the maximum, reducing system size and design complexity and lessening unstable factors that may generate interference and error should be considered, which are as well as the core idea of the entire design of the collection system.

The sampling rate of the A/D conversion system used to collect single fast pulse must be in GHz order, then the change frequency of digital signal output after conversion should also be in GHz order. There are hardly any devices available in the field of electrical signal to conduct parallel-serial conversion at such a high speed and furthermore the problem of intact signal may be caused for the design of the system. In accordance with the design target in the course of transmission, the scheme adopted by us is "speed reduction—storage in cache", "fast storage—slow withdrawal", that is, to store in cache the data in GHz order into the storage unit such as FPGA chip, then read the data at the speed of 50—100 MByte/s via logical control and finally conduct parallel-serial conversion.

3 System design scheme

To collect single fast pulse, the system designed by us has the main technical parameters as follows:

Sampling rate: 1.2 GSPS

Vertical resolution: 8 bits

Input bandwidth: 1 GHz or above

Number of sampling points: 4096 points or above

Figure 2 is the principle diagram of system design while the working principle of each part in the system has been described in the text above. The attenuation fan-out module in signal input end divides the measured signal into two roads: one for measurement, and the other for trigger the FPGA internal logic to start the storage the sampling results, so as to realize self-trigger of the signal.

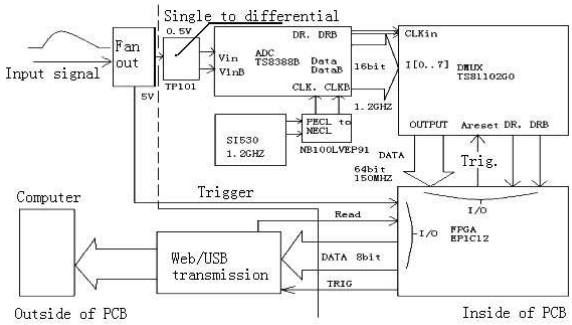

Fig. 2. Principle diagram of collection system

For FPGA, we select to use EP1C12 chip of Altera Corporation to realize the functions required for the system. The detailed design for digital advance sampling inside the chip is as shown in Fig. 3.

TS8388B of Atmel Corporation is selected to be our core A/D chip[4]. The chip is a kind of 8-bit ADC, with full-power bandwidth (3 dB) for analog signal being 1.5 GHz and sampling rate up to 1 G above. In the differential input mode, the dynamic range at the input end is from +250 mV to −250 mV. DSPLL model clock chip SI530 from SILICON LABORATORIES is adopted by the system to directly generate differential clock signal of 1 GHz above, so as to provide ADC chip with sampling clock.

Digital branch switch chip (DMUX) TS81102G0 manufactured by Atmel Corporation, which is used matching with TS8388B, is used to perform frequency reduction[5—8]. When digital signal arrives, matching with the action of clock input, the input signal is latched to level-1 latch register of A—H channel in turn; at the time when data has been latched to H channel, the system shall send action command to simultaneously transfer the data in the eight channels to level-2 latch register; then, the data is output matching with the time sequence of output clock[9—13].

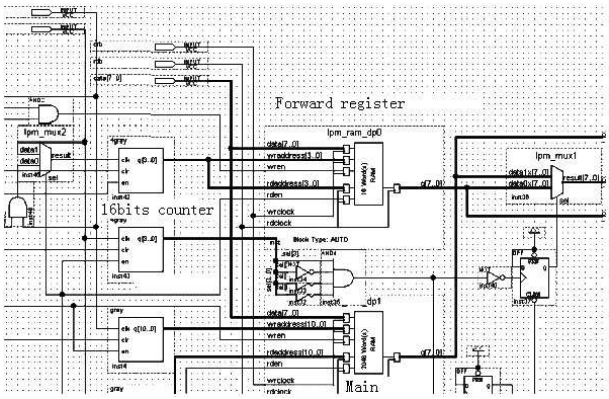

Fig. 3. Logic module design for advance sampling (the part of prefix register).

The simulation results of the design is shown in Fig. 4, with the write clock and read clock of simulation set to be 200 MHz and 50 MHz respectively, storage capacity of prefix register set to be 16Byte and the input signal being one Gray counter of the output. As shown in Attached Drawing 4(a), the trigger arrives when at the moment when "34" is counted. However, as we can find in Attached Drawing 4(b), 16 data before the moment of trigger is still readable except for the occurrence of transient errors to one data during the corresponding time of period due to switch action at the moment of chip select. If more advanced devices of Altera Corporation, such as Stratix GX series, are adopted, the duration of this error data shall be shortened and the frequency of write clock recognizable for the system shall also be raised to 500 MHz above.

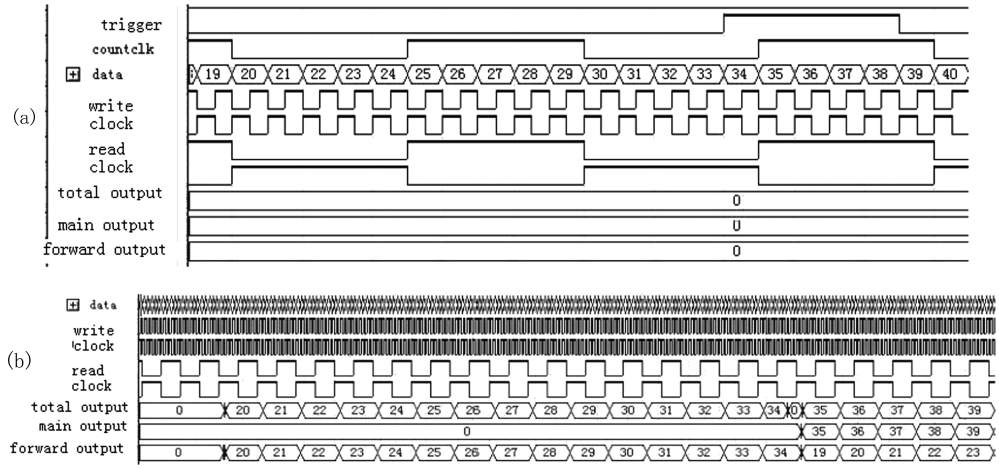

Fig. 4. Simulation results of advance sampling. (a) time sequence of the system before trigger signal arrives; (b) time sequence at the beginning of the time when data are read.

Our design puts the electrical-optical conversion part on printed circuit board bearing core devices and we use TLK1501 of Texas Instruments (TI) as parallel-serial converter and HFBR-5921L of Agilent Technologies as fiber optic transceiver to convert 8-bit signal output via FPGA to optical fiber signal in parallel. Since the two types of chips possess bidirectional function, optical-electrical conversion part at the receive end 1.5 kilometers away still adopts HFBR-5921L and TLK1501 optical fiber collection card to convert the signal transferred by optical fiber to 8-bit signal. At the receive end, data is transferred into the computer through USB interface. Finally, softwares such as matlab or labviewcan are used to restore the digital signal acquired to the waveform of original analog signal[14—16].

4 Analysis on tested results and scheme for improvement

A step signal with rise time of 10 ns is input at the input end by us, and the rise time is collected and restored, with the final results shown in Fig. 5.

From the restored results as shown in the Figure, we can see the trend of step signal, but the signal quality is very poor with a large number of burrs. These noises of the system are mostly digital switch noises. Since there is a 0 ohm resistance in the connection between digital and analog ground planes in the system, the digital switch noise is coupled into

the analog circuit, which makes the input signal to be so interfered as to generate a large number of burrs. In the former system design, the digital and analog ground planes are connected by ferrite bead, which is a equivalence to electrical inductor that can separate high-frequency digital noise. However, a voltage difference of 0.5 V shall be generated on the ferrite bead due to the rapid change of digital current in the system, which may further lead to unequal level between the digital and analog ground planes, the unsatisfactory analog power voltage and abnormal work of ADC. Therefore, to realize the system functions, resistance is chosen to connect the digital and analog ground planes for the moment, and in the future ferrite bead with appropriate inductance value should be chosen to improve the functionality of the system[17, 18].

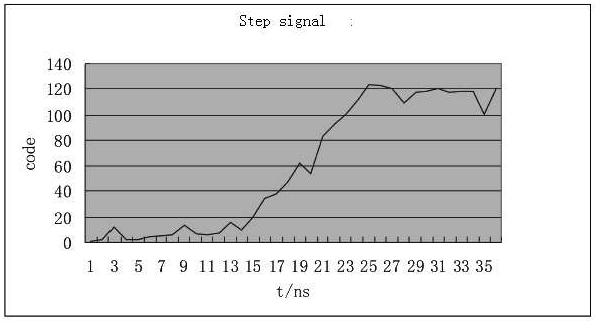

Fig. 5. Restored results of step signal.

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