A Digital Control Scheme of Power Supply System for RCS/CSNS

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Abstract A 1.6GeV proton rapid cycle synchrotron (RCS) was designed in the Chinese Spallation Neutron Source (CSNS) Project. The magnet power supply system of the synchrotron drives nine sets of independent 25Hz White Circuit. The output currents of the nine sets of magnet power supply are the DC-biased AC source. The currents (magnetic fields) must meet the requirements of the phase and amplitude accuracy during the accelerator repetition cycle. Because of the advantages of the digital control technique such as reliability, temperature drift rejection, and high integration and so on, it has been adopted more and more widely in the equipment design. To achieve the rigorous goals such as stability and THD (Total Harmonic Distortion) in the RCS/CSNS magnet power supply system, a digital control scheme will be implemented which will be presented in this paper.

Key words White Circuit, power supply system, stability, total harmonic distortion, digital control

1 Introduction

There are seventy-two magnets in the RCS and they are divided into nine families shown in Table 1: one for the bending magnets (BM) and eight for the quadrupole magnets (QM), and nine sets of power supply are employed for exciting these magnet families respectively. According to the beam dynamics, the tracking error of the magnet exciting current (magnet field) among the nine magnet families should be less than 0.1%.

Table 1. Magnets classification in RCS.

magnet type		number
bending magnet	BM	24
quadrupole magnet	QFC1	8
	QFC2	8
	QFC3	4
	QD	8
	QF	8
	QDG	4
	QFG	4
	QDC3	4

2 Configuration of the power supply system

The specifications for the power supply output current could be deduced from the requirements of 0.1% magnet current tracking error among the nine magnet families, and are listed below:

1) Amplitude stability better than 0.1%;

2) Phase error less than 10μs;

3) Frequency stability better than 0.01%;

4) THD (Total Harmonic Distortion) less than 0.02%.

2.1 White Circuit[1]

White Circuit is widely used in RCS magnet power supply system, because the power supply is only burdened with the elements active loss while the reactive power flows between the magnets and the energy-storage elements, which avoids a huge throughput on the power lines. The output power of BM power supply is about 2.7MW. For the sake of

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feasibility and reliability, the BM power supply will be designed with AC and DC power supply separately. The schematic of 24 meshes BM resonant network with separated AC & DC power supplies is shown in Fig. 1.

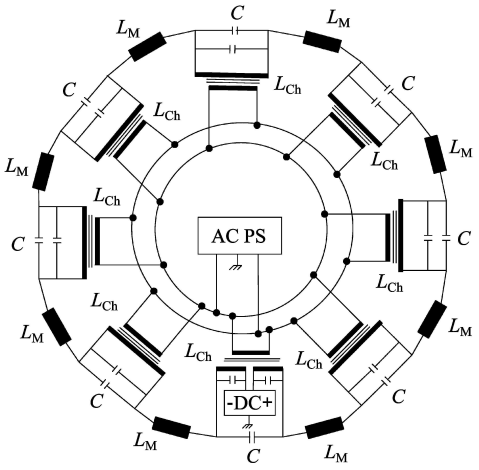

Fig. 1. Schematic of White Circuit for BM.

The total power of eight sets of QM power supply is about 4.0MW. For the sake of the phase synchronization, the eight sets of power supplies are designed with AC and DC power supplies combined shown in Fig. 2.

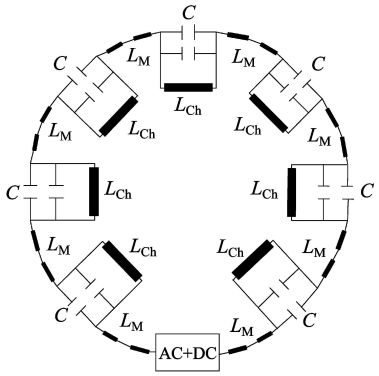

Fig. 2. Schematic of White Circuit for QM.

2.2 The operation mode of White Circuit

The output behavior of the current in all of the magnets has the same expression, only the amplitudes of DC ($I_{\rm DC}$) and AC ($I_{\rm AC}$) are different for the different magnet family.

$$i_{\rm Magnet} = I_{\rm DC} - I_{\rm AC}\cdot\sin\omega t = I_{\rm DC} - I_{\rm AC}\cdot\sin(2\pi\cdot 25\cdot t). \tag{1}$$

The proton will be injected into the RCS at the valley current and extracted at the peak current. The RCS may operate in different modes, for instance, the energy of the proton may be 80MeV, 1.4GeV and so on. The power supply should have the corresponding operation modes. In other words, the amplitude $I_{\rm DC}$ and $I_{\rm AC}$ could be set flexibly in this range.

3 The digital control scheme of the magnet power supply system

In order to satisfy the flexible operation mode, the AC and DC references will be designed individually. The sinusoidal reference will be designed as a look-up table in the digital control system. Each power supply has its own current regulator. The current error between the reference and the feedback is input to the digital regulator for current regulation. The precise 25Hz reference from the Control Center and the phase error are inputs of the DC-biased 25Hz AC reference generator to ensure the phase synchronization.

3.1 Current regulation

The high precise stable DC current power supply has been realized in BEPC II [2], so the crux is the control of the AC current.

With the multiple operation modes of the power supply system and the convenient implementation of the hardware such as FPGA taken into consideration, the schematic of single power supply current regulation is shown in Fig. 3.

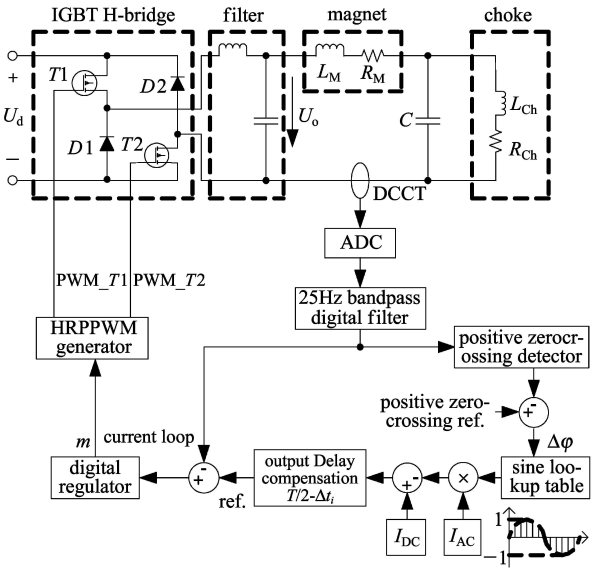

Fig. 3. The DC-biased AC current regulation.

Suppose "$U_{\rm d}$" is the input of the IGBT H-bridge type converter and "$U_{\rm o}$" is the output of the inverter after being filtered and "m" $(-1<m<1)$ is the modulation coefficient for duty cycle. Then the current in the magnet is:

$$i_{\rm Magnet}=U_{\rm o}/(R_{\rm M}+R_{\rm Ch})=mU_{\rm d}/(R_{\rm M}+R_{\rm Ch}). \quad (2)$$

Where $R_{\rm M}$ is the resistance of the magnet and $R_{\rm Ch}$ is the resistance of the choke.

It shows that m has the same change law as the current in the magnets. Because the BM power supply has an individual DC regulation loop so $I_{\rm DC}$=0 here.

3.1.1 The positive DC-crossing detector

The current waveform positive DC-crossing point is chosen as the phase error ($\Delta\varphi$) detecting point because the current change rate ($\mathrm{d}i/\mathrm{d}t$) is the largest at this point. It means that tiny phase error will lead to large current error that can be detected easily. The Control Center provides a precise 25Hz reference clock and the phase will be adjusted once during a repetition cycle (40ms). Given the power supply receives the precise 25Hz reference clock at the time t=0ms, then the phase error sampling time is at t=20ms, 60ms, 100ms and so on.

To filter the phase error introduced by the disturbance of direct current, the AC current error should be the difference of the current error at the corresponding sampling point and the direct current error, which is the difference of the average sampling current and $I_{\rm DC}$ reference.

3.1.2 The output delay compensation

There is a system intrinsic delay for every power supply, defined as the delay between the reference input and the output response. The intrinsic delay is likely to be different among the nine sets of power supply, and we must compensate this difference. Suppose Δt_i is the intrinsic delay time of the ith power supply, a delay function block of $T/2-\Delta t_i$ is inserted for the current reference, and then the total delay is $T/2$ (20ms). It means all the nine sets of power supply have the same response outputs after a total delay of $T/2$.

3.1.3 The digital regulator

The digital regulator should implement the following functions for the DC-biased AC current:

1) A suitable gain at very low frequency to ensure that the DC component gets a gain and the system is stable as well;

2) A reasonable high gain for AC component at the frequency of 25Hz.

The possible transfer function that meets the two requirements above in S-domain is:

$$H(s)=\frac{k_0(1+k_1s)(1+k_2s)(1+k_3s)}{s(s^2+2\xi\omega s+\omega^2)}. \quad (3)$$

Where ξ $(0<\xi<0.707)$ is the damping ratio, and ω $(\omega=2\cdot\pi\cdot25)$ is the resonant angular frequency at 25Hz, and k_0 is the gain for the regulator, and $k_i=(2\cdot\pi\cdot f_i)^{-1}$, and f_i is the ith corner frequency for the regulator.

The bode diagram is shown in Fig. 4.

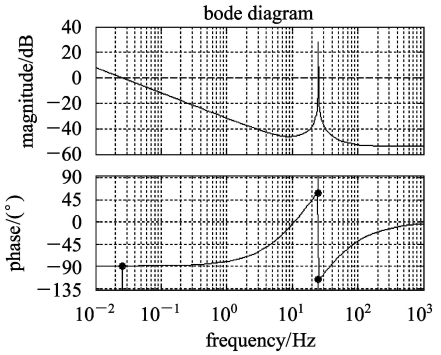

Fig. 4. The bode diagram of digital regulator.

3.1.4 The HRPPWM generator

The aim of the HRPPWM is to generate a series of pulse whose width being converted from the modulation coefficient m to drive the IBGT H-Bridge. Given the switching frequency of the IGBT is 20kHz and the system clock of the FPGA is 100MHz, suppose the modulation coefficient is m=0.7, then the number of resolution intervals contained in the driving pulse (duty cycle) is: 100MHz/20kHz·0.7=3500.

In other words, when a counter is used, it means there will be 3500 system clocks during a Pulse-Width Modulation (PWM) period (1/20kHz=0.05ms).

To get a high regulation precision PWM (HRPPWM), the fractional of one resolution interval will be reserved after rounding correction and will be

added to the input for the next PWM period. When the sum is greater than one resolution interval, then an additional pulse will be added to the normal PWM generator, and so on. This principle of this method is similar to PFM (Pulse Frequency Modulation). The block diagram is shown in Fig. 5.

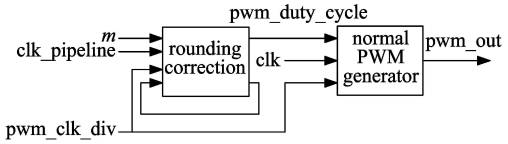

Fig. 5. The block diagram of HRPWM generator.

The algorithm is based on the reference-follower design. Just the current regulation loop is adopted because of the nonlinearity of the magnet inductance (1%). While the relation between the voltage (U_{Magnet}) and current (i_{Magnet}) of the magnet is:

$$U_{\mathrm{Magnet}} = L\mathrm{d}i_{\mathrm{Magnet}}/\mathrm{d}t. \tag{4}$$

It means the voltage and current cannot be sinusoidal wave at the same time. While what we need to adjust is the current, so the voltage regulation loop will not be used here.

3.2 The pase regulation

Suppose the first injection and extraction period is shown in Fig. 6 and the feedback current lags the reference, and then the second reference starting point should be higher than the first one to compensate the phase lag. Also for the sake of tolerance of the power devices, the next starting point should not jump too high, and it means a jump-step limit should be used here.

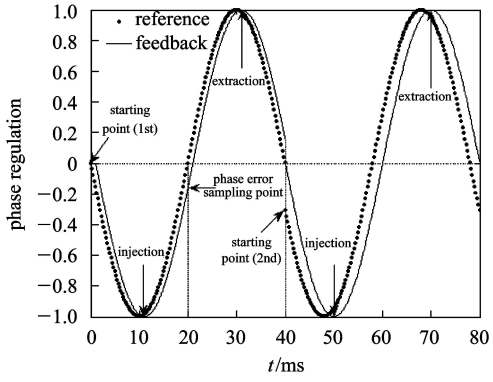

Fig. 6. The phase regulation.

The $\Delta\varphi i$ ("i" from 1 to 9) determines the starting point of the next period cycle (40ms) for sine reference i, and the precise 25Hz reference from the Control Center determines the starting time for synchronization. The full control system is shown in Fig. 7.

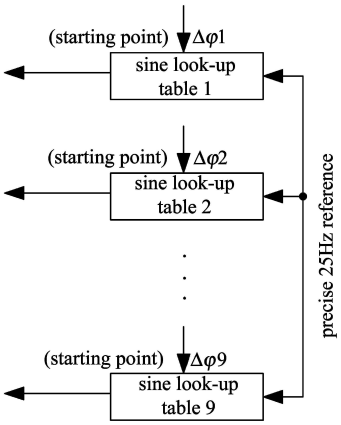

Fig. 7. The full control of power supply system.

Here we do not intend to take the BM current as the phase reference as the tradition[3, 4] did because the generation of the real-time look-up table will burden the FPGA, also the disturbance of the BM current such as the noise may lead to unnecessary regulation to the QM power supply.

4 Simulation

The simulation diagram for Fig. 3 is shown in Fig. 8, which is based on Matlab/Simulink.

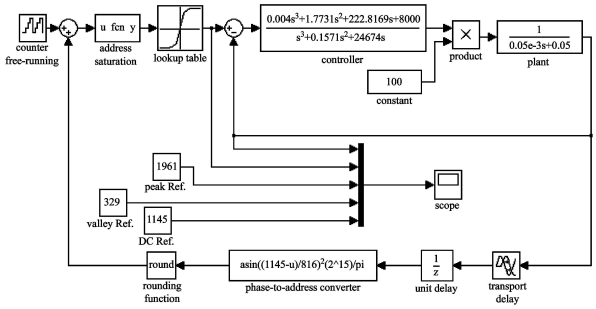

Fig. 8. The simulation of digital control for power supply.

The simulation result is shown below (Fig. 9):

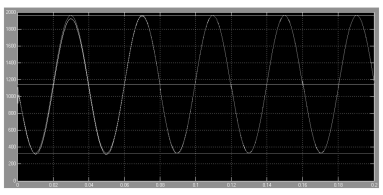

Fig. 9. The simulation result.

It shows that the digital control loop works well.

5 Summary

This paper proposes a digital control scheme for the nine sets of magnet power supply system for RCS/CSNS. The feasibility will be verified when the power supply model is built up in the middle of this year.

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中国散裂中子源/快循环同步加速器电源系统数字化控制方案

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摘要 在中国散裂中子源工程中, 需要设计1台1.6GeV快循环同步质子加速器. 加速器的磁铁电源系统驱动9套怀特电路. 这9套电源的输出都是带直流偏置的交流电流源. 在每个重复加速周期内, 电流(磁场)必须保证相位和幅值精度. 数字控制技术的可靠性、温度漂移抑制、高集成性等等使得它在越来越广泛地应用于控制电路的设计中. 为了达到中国散裂中子源电源系统苛刻的指标, 本文提出了一种数字化控制方案.

关键词 怀特电路 电源系统 稳定度 总谐波失真 数字控制

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